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Seven Level Inverter Based Shunt Hybrid Active Power Filter Topology for Harmonic Reduction

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ABSTRACT: This paper presents a three-phase asymmetric cascaded seven level inverter (ACSLI) based Shunt Hybrid Active Power Filter (SHAPF) topology for harmonic reduction in medium voltage test system (MVTS). The proposed SHAF topology consists of ACSLI based shunt active power filter (SAPF) and shunt passive filters (SPF) connected in parallel with the load. The SHAPF topology compensates harmonic currents drawn by non-linear load. The compensation process is based on concept of synchronous reference frame theory (SRFT) used for reference compensation current estimation, carrier switching frequency sub-harmonic pulse width modulation (CSFSHPWM) for generating switching signals for ACSLI, fuzzy logic controller (FLC) for maintaining DC bus capacitor voltage constant. Three types of shunt passive filters namely single tuned, double tuned and high pass filter are used individually for enhancing the harmonic filtering performance of ACSLI based SAPF. The proposed SHAPF topology is validated through MATLAB/SIMULINK simulation for MVTS and the results were presented.

Key words: Asymmetric cascaded seven level inverter, Shunt hybrid active power filter, Synchronous reference frame theory, Fuzzy logic controller, Shunt passive filter.

I. INTRODUCTION

The usage of nonlinear loads at high voltages is increasing in industry day-by-day leading to harmonic pollution in the line current, increased losses, poor system performance and efficiency. The conventional two level active filters have limitations in medium and high voltage applications due to semiconductor reverse voltage rating constraint, high power loss, high level of dv/dt causing switching noise hence electromagnetic interference with communication system, as well as insulation degradation in electronic and electrical systems [1]. The development of multilevel inverter (MLI) has become the option for reactive power compensation and power quality improvement. Multilevel inverter topologies such as diode clamped, flying capacitor and cascade H-bridge inverters are available in the literature [2]. Out of these topologies cascade multilevel inverter requires less number of components to produce same number of levels [3]. Cascaded inverters are modified to asymmetric cascaded multilevel inverter (ACMLI) topologies to reduce number of switches with each DC source driven at different voltage level [4]. Defining 'S' as the cell number and n=1,2,…S, the ACMLIs are classified as MLI with$(2^{S-n})* V_{DC}$ factor and with $(3^{S-n})*V_{DC}$ factor . In this paper MLI with $(2^{S-n})* V_{DC}$ factor is used as SAPF. In this configuration the magnitude of DC voltage sources will increase by a factor (2^{S-n}). The output waveform has number of levels equal to $(2^{S+1} -1)$[5]. In active power filter application there is no need of active power output from the inverter, therefore a separate DC source for each converter bridge is not required. Hence in this paper single DC source is used and the other storage device is replaced by a capacitor.

II. OPERATION OF ACSLI BASED SHAPF

The test system with ACSLI based SHAPF compensation is shown in Fig.1. It consists of a three phase medium voltage AC source connected to nonlinear diode rectifier load through a line. An ACSLI based SAPF and shunt passive filter are connected in parallel with the load. In the operation of APF, the harmonic component of load current is derived through harmonic detection circuit and reverses it as the reference compensation current. Then switching signals for ACSLI are generated such that AC side output current of APF correctly traces reference current and provides the harmonic current of the load, so that source current will be free from harmonics and approaches towards sinusoidal. In addition to SAPF, SPF is connected in parallel with the load to bye-pass some selected harmonics so that burden on active filter reduces and its filtering performance increases.

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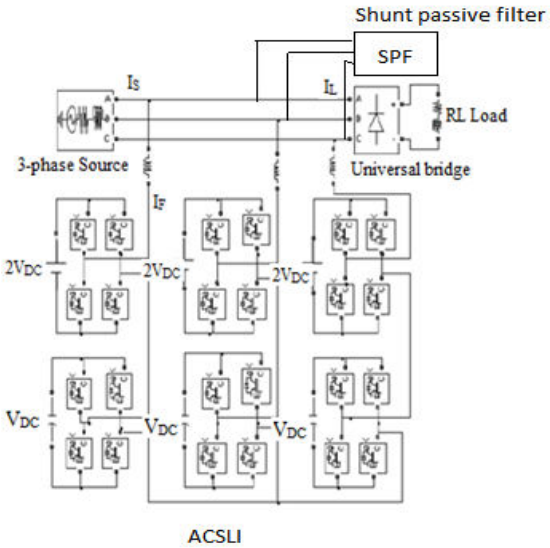

Fig1.Medium voltage test system with SHAPF compensation.

III. SIMULINK MODEL OF MVTS WITH PROPOSED ACSLI BASED SHAPF COMPENSATION

The SIMULINK model of the test system with proposed ACSLI based SHAF compensation is depicted in Fig. 2.

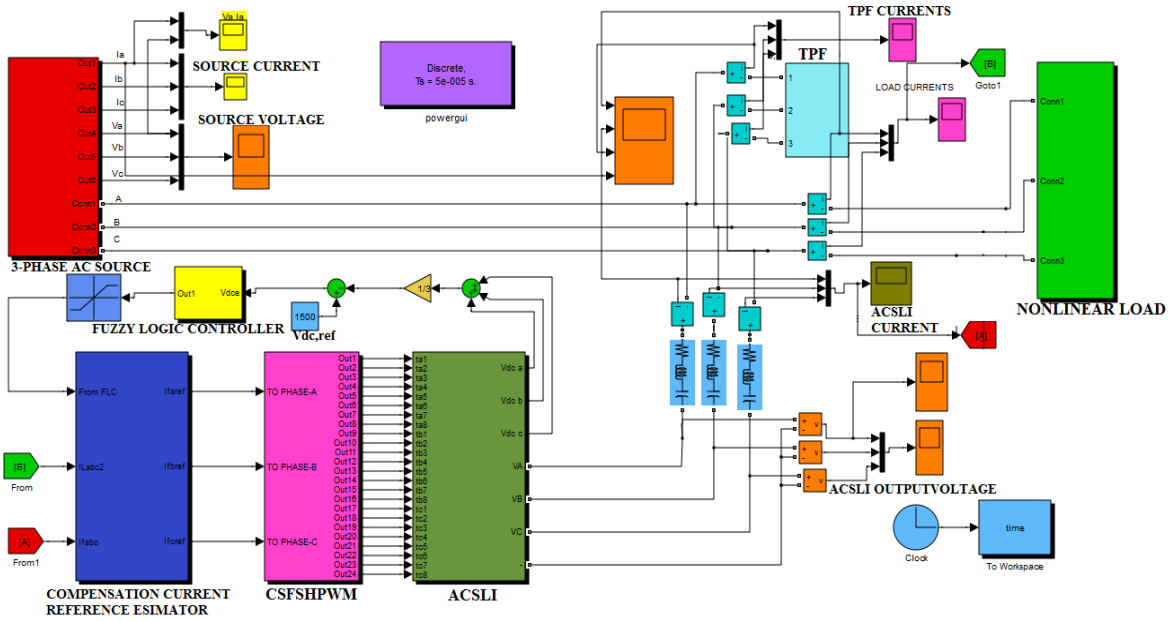

Fig. 2 Simulation model of test system with proposed 7-level SHAPF compensation.

The test system consists of a three phase AC source of voltage 4500 V(peak) and 50 Hz frequency connected to a nonlinear diode rectifier load through a source and line combined reactance of 15mH/phase. The R-L load on the DC side of diode rectifier is 20 ohm and 0.1 mH.

A. Three Phase ACSLI

The three phase ACSLI consists of two H-bridge cells namely low voltage (LV) cell of 1.5kV and high voltage (HV) cell of 3kV connected in series. Each H-bridge cell is constructed using four IGBTs with anti-parallel diodes. Since

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V_{HV} is two times V_{LV}, it can produce seven levels in its output wave form via +4.5kV,3 kV,1.5 kV,0,-1.5 kV,-3 kV and -4.5 kV. A DC source of 3 kV is used as storage device in HV cell and a capacitor of 4000 µF is used on the DC side of LV cell. The DC-bus capacitor value is taken large enough to minimize the variation of its voltage based on the general principle that capacitor load time constant to be ten times to that of fundamental period [5].

B. Control Strategy of ACSLI

The control strategy of ACSLISAPF includes SRFT for estimating reference compensating current, CSFSHPWM for generating gating signals and FLC for maintaining LV cell capacitor voltage constant.

1) Synchronous reference frame theory (SRFT): The time domain methods namely instantaneous reactive-power theory and Synchronous reference frame theory (SRFT) are most commonly used for estimating reference compensating current [6]. SRFT transforms the three phase system voltage and current variables into a stationary reference frame using Park's transformation. The active and reactive components of the three-phase system are represented by the direct and quadrature components respectively. The fundamental components are transformed into DC quantities which can be separated easily through filtering. The system with this technique is very stable since the controller deals mainly with DC quantities and the computation is instantaneous [7]. Suppose the three phase AC source currents are I_{sa},I_{sb},I_{sc}, non-linear load currents are I_{La},I_{Lb},I_{Lc} and active filter compensating currents are I_{fa},I_{fb},I_{fc}. The load currents in a-b-c reference frame can be converted in to d-q reference frame using Park's transformation as shown in equation (1)

$$\begin{bmatrix} I_d \\ I_q \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} \cos\theta & \cos\left(\theta - \frac{2\pi}{3}\right) & \cos\left(\theta + \frac{2\pi}{3}\right) \\ \sin\theta & -\sin\left(\theta - \frac{2\pi}{3}\right) & -\sin\left(\theta + \frac{2\pi}{3}\right) \end{bmatrix} \begin{bmatrix} I_{La} \\ I_{Lb} \\ I_{Lc} \end{bmatrix} \quad (1)$$

These currents can be decomposed into DC component and harmonic component as shown in equation (2).

$$I_d = I_{ddc} + I_{dh}, \qquad I_q = I_{qdc} + I_{qh} \quad (2)$$

The harmonic component of load current is obtained by using a low pass filter and subtracting output of LPF from total load current as shown by eqn. (3).

$$I_{dh} = I_L\text{-LPF}(I_d), \quad I_{qh} = I_L\text{-LPF}(I_q) \quad (3)$$

These reference currents are transformed into a-b-c coordinates by applying Inverse Park's transformation as shown in eqn. (4).

$$\begin{bmatrix} I_{fa}^* \\ I_{fb}^* \\ I_{fc}^* \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} \cos\theta & \sin\theta \\ \cos\left(\theta - \frac{2\pi}{3}\right) & -\sin\left(\theta - \frac{2\pi}{3}\right) \\ \cos\left(\theta + \frac{2\pi}{3}\right) & -\sin\left(\theta + \frac{2\pi}{3}\right) \end{bmatrix} \begin{bmatrix} I_{dh} \\ I_{qh} \end{bmatrix} \quad (4)$$

The SIMULINK model of SRFT used to estimate reference compensating current is shown in Fig. 3. The cut –off frequency of low pass filter is selected as 75 Hz.

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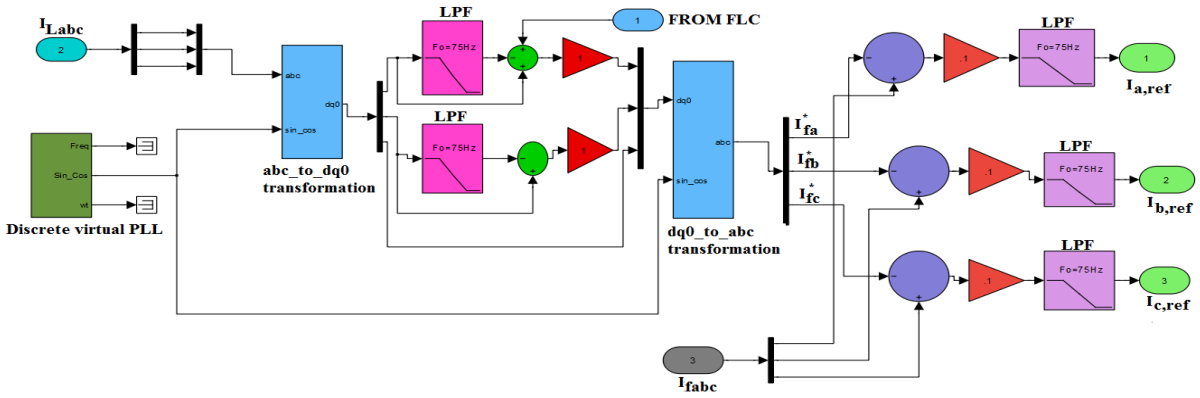

Fig. 3 SIMULINK model of SRFT based compensating reference current estimator.

2) Carrier switching frequency sub-harmonic PWM: Most commonly used modulation techniques for MLIs are Selective harmonic elimination method[8], Space vector PWM method and Carrier based PWM methods[9,10], out of which CSFSHPWM is used in this paper due to its fast response, simple computation and its suitability for MLIs. The MATLAB/SIMULINK model of CSFSHPWM for Phase–a is illustrated in Fig. 4. In this technique six triangular signals each of 2 kHz frequency(f_c) and magnitude(A_c) of 0.33 and displaced vertically are used as carrier signals and the sinusoidal voltage wave form obtained from compensating reference current estimator is used as modulating signal as shown in Figure. 5. The reference waveform has peak to peak amplitude A_m, the frequency f_m, and its zero centered in the middle of the carrier set. The reference is continuously compared with each of the carrier signals. If the reference is greater than "s" carrier signal, then they active device corresponding to that carrier is switched off. In multilevel inverters, the amplitude modulation index "M_a" and the frequency ratio "M_f" are defined as

$$M_a = A_m / (m-1) A_c \quad \text{and} \quad M_f = f_c / f_m \tag{6}$$

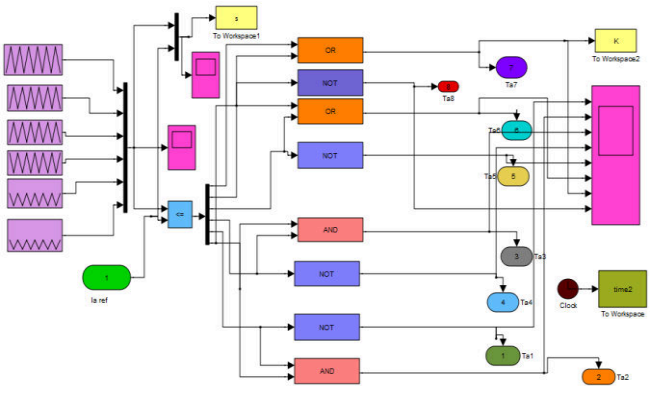

Fig. 4 SIMULINK model of CSFSHPWM for Phase –a.

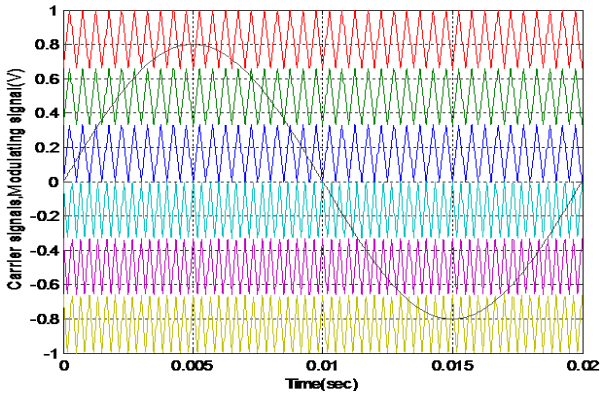

Fig.5 Carrier and reference signals of CSFSHPWM for P hase-a.

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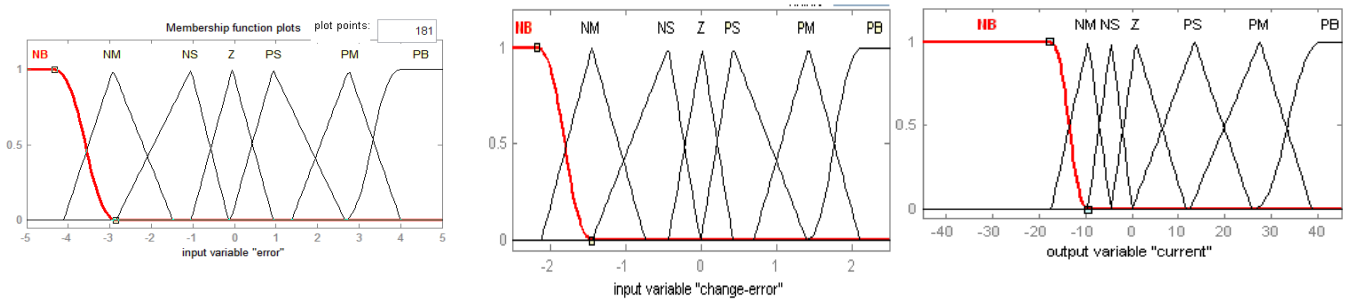
3) Fuzzy Logic based LV cell DC Voltage Controller: Various types of controllers like Proportional-Integral (PI), adaptive, Neuro and Fuzzy Logic Controller (FLC) for DC bus voltage regulation are well presented in literature [11]. Since the fuzzy control rules are not derived from a heuristic knowledge of the system behavior, neither precise mathematical model nor complex computations are needed and is based on human like linguistic terms in the form of IF-THEN rules to capture the non-linear system dynamics, FLC is adopted in this paper to control LV Cell DC bus capacitor voltage. The LV cell DC bus voltage is compared with reference voltage of 1.5 kV to generate error signal. The error and its derivative are applied to FLC to obtain control signal which in turn applied to reference compensating current estimator to control the gating signals of VSI to maintain constant DC bus capacitor voltage at LV cell.



6 (a) 6(b) 6(c)

Fig. 6 The degree of membership functions for (a) The error (b) The derivative of error and (c) The output.

The two inputs and the output of FLC use seven triangular membership functions namely Negative Big (NB), Negative Medium (NM), Negative Small (NS), Zero(ZE), Positive Small (PS), Positive Medium(PM), Positive Big(PB). The membership values of input and output variables are shown in Fig. 6. Each input has seven linguistic variables, therefore there are 49 input label pairs. A rule table relating each one of 49 input label pairs to respective output label is given in Table 1. The type of fuzzy inference engine used is Mamdani and the Centroid method is used for de-fuzzification.

TABLE.I FUZZY RULE REPRESENTATION

e / de	NB	NM	NS	ZE	PS	PM	PB
NB	NB	NB	NB	NB	NM	NS	ZE
NM	NB	NM	NM	NM	NS	ZE	PS
NS	NB	NM	NS	NS	ZE	PS	PM
ZE	NB	NM	NS	ZE	PS	PM	PB
PS	NM	NS	ZE	PS	PS	PM	PB
PM	NS	ZE	PS	PM	PM	PM	PB
PB	ZE	PS	PM	PB	PB	PB	PB

C. Shunt Passive Filter (SPF) :

It is connected in parallel with the load to eliminate the effect of some selected harmonics. Three types of shunt passive filters namely single tuned filter, double tuned filter and high pass filter are used whose configurations are shown in

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Figure. 7. In first case the SPF is constructed by using two single tuned passive filters connected in parallel in each phase and tuned to absorb 5th and 7th harmonic currents in the load current. The 5th order filter consists of a series R-L-C branch with a capacitor (C_5), inductance (L_5) and resistance (R_5) and 7th order filter consists R_7, L_7 and C_7 in series. Quality factor of the filter is selected as 75 and the filter capacitance value is fixed at 30µF[12]. The parameter values of the single tuned passive filter are R_5=0.2829Ω, L_5=13.504 mH, C_5 =30µF, R_7= 0.2021Ω, L_7= 6.892 mH and C_7 =30µF.

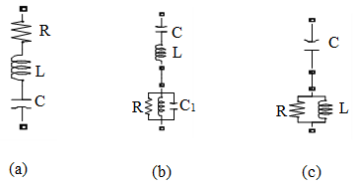

Fig. 7 Passive filter configurations (a)Single tuned filter(b) Double tuned filter and (c)High pass filter.

Design parameters of double tuned filter for absorbing 5th and 7th harmonic currents obtained at Q = 75 are C=30µF, L=9.64mH and R= 1344.65ohms. Design parameters of high pass passive filter at Cutoff frequency=50Hz and Quality factor of 75 are C = 30µF, R=70.73ohms and L=2mH.

IV. RESULTS AND DISCUSSION

The simulation results of MVTS without any compensation are presented first, followed by basic ACSLI based SAPF compensation and the proposed ACSLI based SHAPF compensation. The performance of ACSLI based SAPF and ACSL based SHAPF with different passive filters for mitigating harmonics in MVTS is compared.

A. Results of MV Test System without any compensation

As can be seen in Fig. 8(a), that the current drawn by diode rectifier load is highly distorted and deviated significantly from sinusoidal waveform due to which the source current and source voltages are also distorted as shown in Figs.8(b) and 8(c).

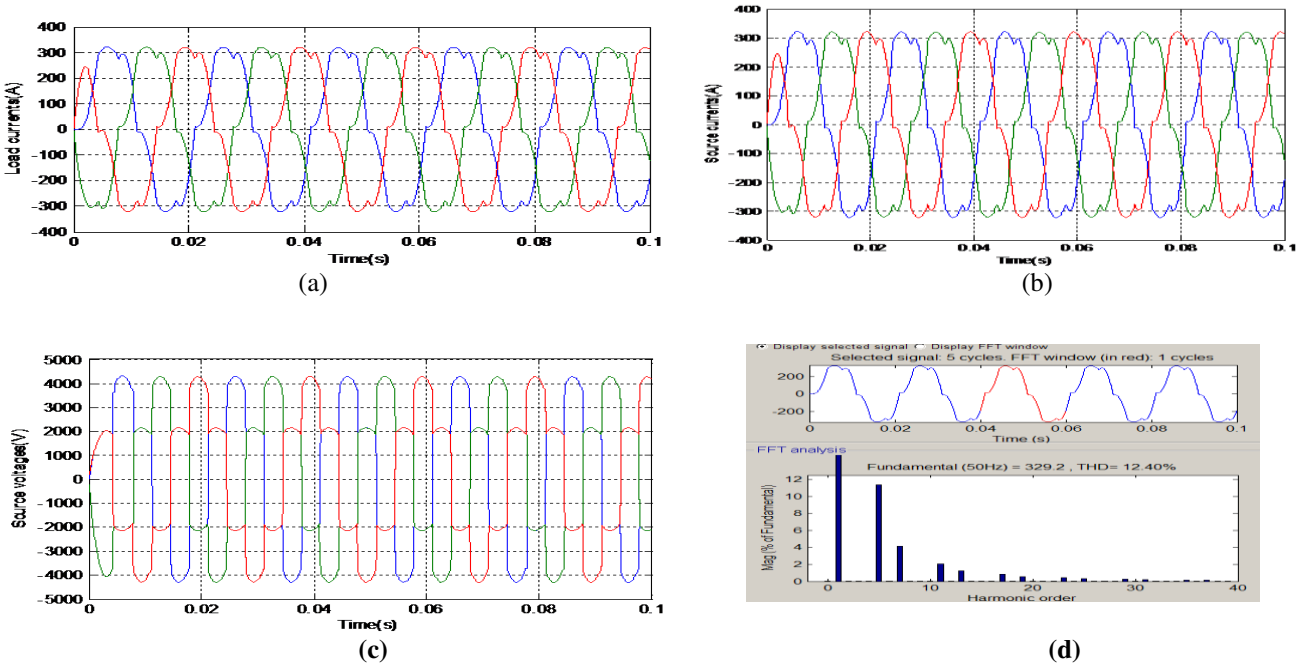

Fig.8 Simulation results of MV test system without compensation a) Nonlinear load currents b) Source currents c) Source voltages d) THD analysis for source current of Phase-a

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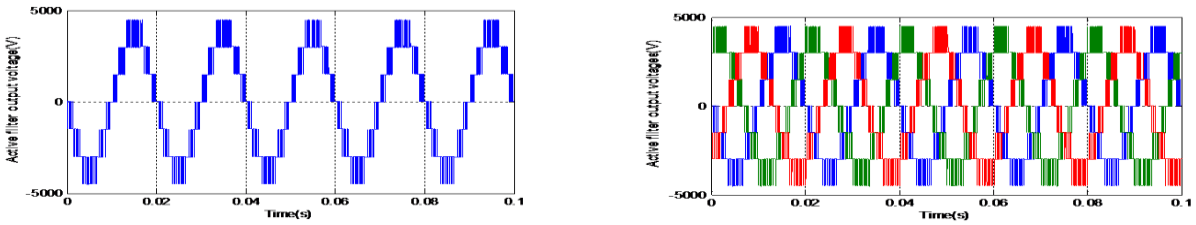
The distortion in the source voltage waveform is due to the presence of source and line inductance and distorted currents drawn by the load. The total harmonic distortion in source current of phase-a without any compensation is 12.4% as shown in the harmonic spectra of Figure 8(d). It is seen that the most dominant are 5^{th} and 7^{th} order harmonics in the spectra plot.

B. Results of MVTS with basic ACSLI based SAPF Compensation

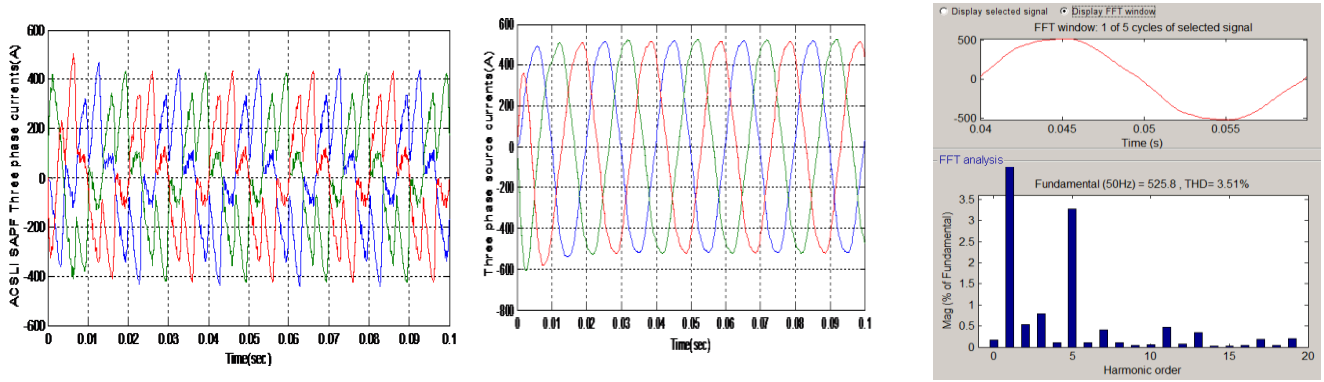
The Fig. 9 shows the single phase and three phase seven level output voltage wave forms of ACSLI based SAPF from which it is evident that CSFSHPWM worked effectively and produced seven levels in the output voltage wave form.



(a) (b)

Fig. 9 Seven level voltages generated by the asymmetric cascaded inverter for (a) Phase-a (b) Phases a, b and c.

The three phase compensating currents of ACSLI based SAPF shown in Fig. 10(a) are effectively compensated the load current harmonics and the source current approached sinusoidal as shown in Fig. 10(b). The THD in source current of phase-a is reduced from 12.4% to 3.51% as shown in Fig.10(c). The ACSLI based SAPF successfully filtered the harmonic current components caused by the nonlinear load. Although the high frequency harmonic components are filtered significantly, appreciable amount of lower order harmonics (5^{th}, 7^{th},11^{th}…..) still remain in the source current spectrum. The most dominant are 5^{th} and 7^{th}order harmonics.



(a) (b) (c)

Fig. 10. (a)Three phase compensating currents of ACSLI based SAPF (b) Three phase source currents (c) Harmonic spectra of source current for Phase-a.

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C. Results of MVTS with proposed ACSLI based SHAPF Compensation

The three phase compensating currents of ACSLI based SAPF and TPF in SHAPF topology are shown in Fig. 11(a) and 11(b). Due to these compensating currents source current became sinusoidal as shown in Fig. 11(c) and its THD is reduced to 1.01% as shown in spectra plot of Fig. 11(d).

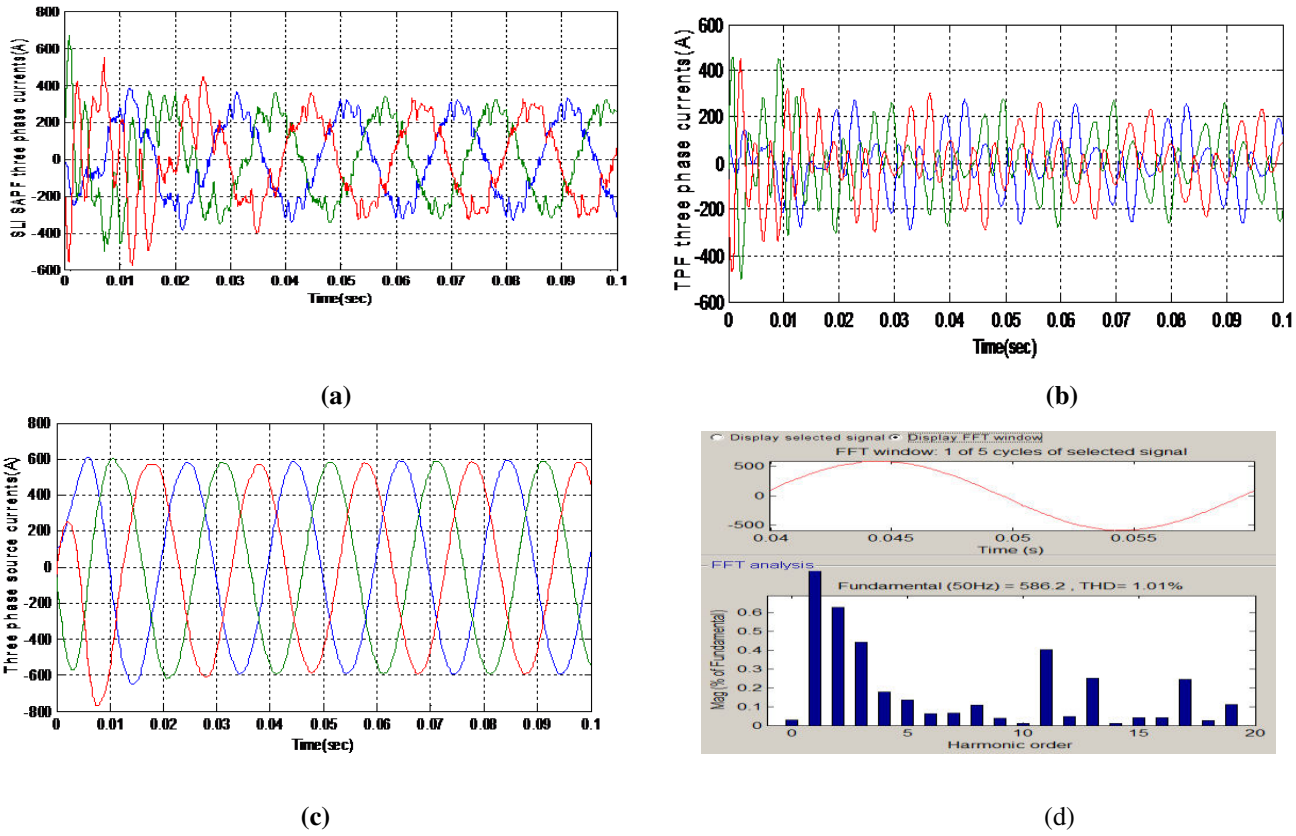

Fig. 11 (a) Compensating three phase currents of ACSLI based SAF (b)Tuned passive filter currents (c) Source current and (d) Harmonic spectrum of source current for Phase-a.

The source current THDs with ACSLI based SAPF and ACSLI based SHAPF compensations with different shunt passive filters are compared in Table II.

TABLE.II COMPARISION OF SOURCE CURRENT THD.

Type of compensation		**THD_i (%)**		
		I_{sa}	**I_{sb}**	**I_{sc}**
Without any compensation		12.4	12.4	12.4
With ACSLI based SAPF Compensation		3.51	3.28	3.44
With proposed ACSLI based SHAPF compensation	With single tuned passive filter	1.01	1.29	1.25
	With double tuned passive filter	2.09	2.04	2.01
	With High pass passive filter	1.84	1.83	1.84

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V. CONCLUSIONS

The SRFT based compensating current estimator worked effectively in estimating compensation current and CSFSHPWM produced switching signals for ACSLI to produce seven levels in the output voltage. Based on the results, the proposed SHAPF topology is capable of responding effectively to the harmonics caused by the three-phase diode rectifier load and compensated the harmonics effectively. The total harmonic distortion of the source current without any compensation is 12.4 % in each phase and it is reduced to 3.51% with ACSLI based SAPF and to 1.01% for phase-a with proposed ACSLI based SHAPF compensation which is fairly good. Thus the performance of SAPF is improved by connecting shunt passive filters in the proposed ACSLI based SHAPF topology.

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BIOGRAPHY

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