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Novel Low Power Logic Gates using Sleepy Techniques

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ABSTRACT: The subthreshold voltage is declining in successive nanometre technologies and has an associated effect of enhanced leakage current. This causes the static (leakage) power to be a vital portion of total power dissipation in a VLSI circuit. Two novel circuit techniques for leakage current reduction in logic gates are presented in this work. The proposed circuit techniques are applied to universal NAND and NOR logic gates. The performance of these low leak gates is compared with earlier CMOS circuit leakage minimization techniques applied to these gates. The novel ultra low leak technique provides maximum leakage current reduction with lower output levels. Low Power State Retention-LPSR technique provides lower leakage power and the state of the gate can also be retained in sleep mode. The proposed low leak gates are designed and simulated using cadence design tools for 90 nm CMOS process technology. The leakage power for the novel methods during sleep mode is found to be better with and without state retention as compared to earlier best known techniques. The dynamic power dissipation for the proposed techniques is least.

KEYWORDS*:* Leakage power, sleep transistor, power gating, total average power, state retention.

I.INTRODUCTION

For successive technology generations the transistor feature sizes are becoming smaller and the channel length is reducing. The threshold voltage and gate oxide thickness are also being scaled down [1] to maintain performance.

The subthreshold voltage is going down to keep pace with reduced supply voltage for scaled down technologies in order to have good performance. The lower subthreshold voltage in nanometre technologies gives rise to enhanced leakage current because transistors cannot be switched off completely. Subthreshold current is the drain to source leakage current when the transistor is off. Leakage current acts as a limiting factor for further scaling down of transistors as per the International Roadmap for Semiconductor Technology (IRST) [2]. Thus it is essential to reduce leakage (static) power consumption during the idle or standby states of the circuits.

When a CMOS circuit is active, the total power dissipation is due to dynamic and static components. In the inactive (standby) mode, the CMOS circuit dissipates power due to the standby leakage current [3] [4]. Sub-threshold leakage current for $V_{GS} < V_T$ is given by

$$I_{DS} = I_{DSO}\, e^{(V_{GS}-V_T)/(nv_T)}[1-e^{(-V_{DS}/v_T)}] \qquad (1)$$

where,

$$V_T = V_{TO} - \eta V_{DS} + \gamma\,[(\phi_s + V_{SB})^{0.5} - (\phi_s)^{0.5}] \qquad (2)$$

In these equations I_{DSO} is current at threshold dependent (on process and device geometry), V_{TO} is the zero bias threshold voltage, γ - is the linearized body effect coefficient, η represents the effect of V_{DS} on threshold voltage, n is the sub-threshold swing coefficient, V_T is thermal voltage respectively. η term describes Drain Induced Barrier Lowering. Subthreshold conduction is enhanced by Drain Induced Barrier Lowering (DIBL) in which positive V_{DS} effectively reduces V_T. Leakage current doubles for every 8^0 to 10^0K rise in temperature.

The subthreshold leakage current can be reduced by increasing threshold voltage V_{TO}, increasing source to substrate potential V_{SB} and reduction of gate to source potential V_{GS} and reduction of drain to source potential V_{DS} and lowering the temperature. Sleepy Transistor[5], Sleepy Stack[6], DRG Cache[7], Gated V_{DD}[8], Sleepy Keeper[9], Multiple Power Gating[10], VCLEARIT[11] are some of the circuit level techniques for low leak operation. Different

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multi V_{TH} techniques for low leak operations discussed in literature are Dual threshold CMOS [12] Variable threshold CMOS (VTMOS) [13].

The techniques discussed above result in either destruction of state or floating output voltage, large dynamic power dissipation, large number of extra transistors etc...

Novel techniques for leakage power reduction to achieve higher leakage power reduction as well as lower total power dissipation with the provision of state retention are proposed in this work. The organization of the work is as follows. Section II deals with performance analysis of some well known leakage reduction techniques applied to gates. Section III deals with novel power reduction techniques for logic gates. The simulation procedure and results are provided in section IV. The conclusion is provided in section V.

II.PERFORMANCE ANALYSIS OF EARLIER LEAKAGE REDUCTION TECHNIQUES

Some of the representative techniques for leakage power reduction with and without state retention are compared in this section. All these techniques are applied to NAND and NOR gates and their functionality as well as power dissipation performance both in static active mode, sleep mode and pulsed dynamic mode of operation are experimentally analysed in cadence design environment using 90 nm technology files and the results are given in section IV. These observations are compared with novel techniques proposed in the next section.

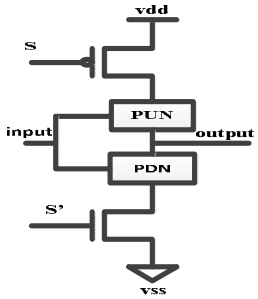

Fig. 1 Sleep Transistor

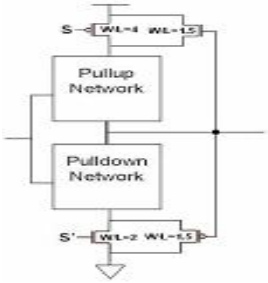

Fig. 2 Sleepy Keeper

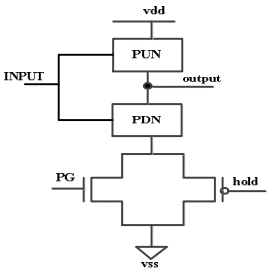

Fig. 3 Multiple Power Gating

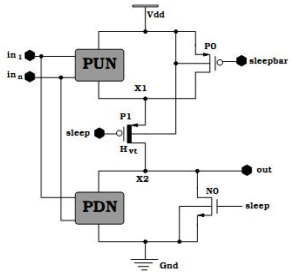

Fig. 4 VLSICT Leakage Reduction

In sleep transistor technique (gated-V_{DD} and gated-GND) technique, pull-up and/or pull-down or both networks are cut off from supply voltage or ground using sleep transistors (figure 1). This approach provides very good leakage power reduction but loses the state information when it enters in to sleep mode. Sleepy Keeper approach introduces additional keeper transistors to the sleep transistor technique to retain the state of the circuit. As has been concluded in this reference this circuit methodology has resulted in large dynamic power dissipation. Multiple power gating method of [10] retains the state but has large associated power consumption. VCLEARIT technique reduces power during sleep mode but results in to large dynamic power dissipation. [14] Has proposed novel techniques to reduce leakage power in inverters with ultra low leak operation and state retention. These techniques are applied to combinational logic gates in this work to achieve better performance.

III.NOVEL POWER REDUCTION TECHNIQUES

Two novel low leak circuit techniques for logic gates are proposed in this section.

- An ultra low leakage power reduction technique with lowest leakage power with lower peak to peak output voltage swing during active mode of operation.
- State retention low leakage technique LPSR with four modes of operation, viz. Active mode , Deep Sleep mode , State Retention with good 1 and State Retention with good 0.

A. Ultra Low Leakage Circuit Technique

The generic block diagram of proposed Ultra Low leak technique is provided in figure 5.

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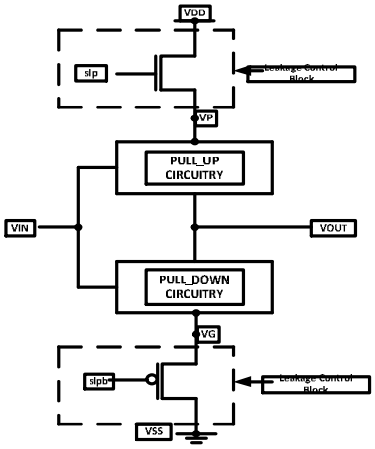

Fig. 5 Block diagram of Ultra Low leakage circuit

The Ultra Low leakage logic gate makes use of PMOS transistor as the pull down sleep transistor and NMOS transistor as the pull up sleep transistor.

- *Active mode of operation*

During active mode of operation the sleep signal slp is held at logic 0 value and sleep-bar signal slpb is held at logic value 1 so that both sleep transistors are on. The node VG is at a higher potential than ground and the node VP is at a lower potential than VDD. The logic gate thus sees lower potential difference across nodes VP and VG. Thus the current though the circuit reduces and power dissipation comes down. The gate has correct functionality but higher logic low and reduced logic high output levels. The power dissipation thus reduces.

- *Standby mode of operation*

During sleep or standby mode of operation the sleep signals are complementary of active mode of operation. Now signal slp is made logic 1 and signal slpb is made logic 0. Sleep Transistors are off, actual power and ground path is broken, the off resistance increases and leakage current is lowered. The virtual ground and virtual power nodes V_G and V_P observe large potentials at their nodes and the potential difference between V_P and V_G is very less. The current flowing through the circuit comes down drastically.

B. Low Power State Retention Technique

The generic block diagram of proposed LPSR technique is provided in figure 6.

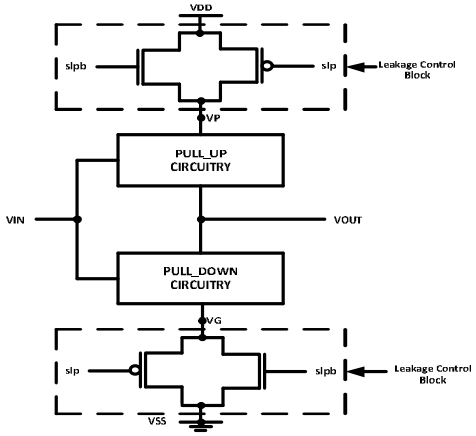

Fig. 6 Block diagram of LPSR circuit

A novel Low Power State Retention (LPSR) circuit technique is proposed in this section. The ultra low leakage gate can be further improved to provide good logic levels during active mode of operation by using a conventional sleep transistor both across pull down and pull up paths of logic gate as shown in fig 6. These transistors help us to obtain good logic levels during active mode of operation.

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State retention novel low leakage gate has four modes of operation:

a. Active mode: both sleep signals are used to switch on the sleep transistors in leakage control block, by making slp=0 and slpb = 1. The node VG is at ground and the node VP is at VDD. The gate thus sees good potential difference across nodes VP and VG. The gate functions as per the truth table.

b. Deep Sleep mode: both sleep signals are used to switch off the sleep transistors in leakage control block by making slp=1 and slpb = 0. Thus the actual power and ground path are broken and the gate experiences lower voltage across the gates; a very high resistance path is established between VDD and ground and the leakage current flowing through the off transistors reduces significantly and hence least power dissipation is observed.

c. State Retention with good 1: The sleep signals are maintained at slp=0 and slpb = 0.The connection to ground is at VG and full VDD is provided. The state retention takes place during sleep mode.

d. State Retention with good 0: The sleep signals are maintained at slp = 1 and slpb = 1.The connection to ground is complete and virtual VDD is provided. During sleep mode the output state is retained.

The states c and d activate one of the sleep control transistors in the pull down path and the pull up path of gate and hence the state of the gate is preserved if there is no change in input values during standby mode of operation.

C. Ultra Low Leakage NAND and NOR Gates

The Ultra Low leakage gates make use of PMOS transistor as the pull down sleep transistor and NMOS transistor as the pull up sleep transistor as shown in fig 7 and fig 8.

During active mode of operation the sleep signal slp is held at logic 0 value and sleep-bar signal slpb is held at logic value 1 so that the two sleep transistors M5 and M6 are on. The node VG is at a higher potential than ground and the node VP is at a lower potential than VDD. The current though the circuit reduces and power dissipation comes down.

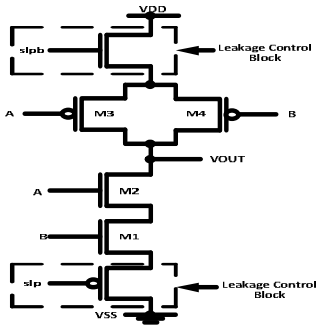

Fig. 7 Ultra Low leakage NAND

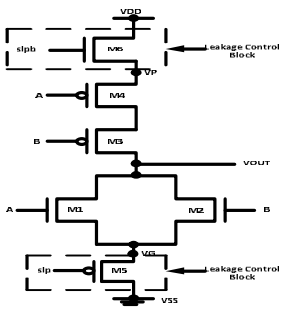

Fig. 8 Ultra Low leakage NOR

During sleep or standby mode of operation the sleep signals are complementary of active mode of operation. For the standby mode of operation the signal slp is made logic 1 and signal slpb is made logic 0. Transistor M5 and M6 are off, actual power and ground path is broken, the off resistance increases and leakage current is lowered due to stack effect.

The ultra low leakage NAND and NOR gates though provides excellent leakage power reduction; the voltage levels at the output are not at good logic1 and logic 0 values. However this larger reduction in leakage power can be utilised in situations wherein very long inactive period of operations are normally encountered and reduced logic levels are acceptable during active mode of operation.

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D. Low Power State Retention NAND and NOR Gates

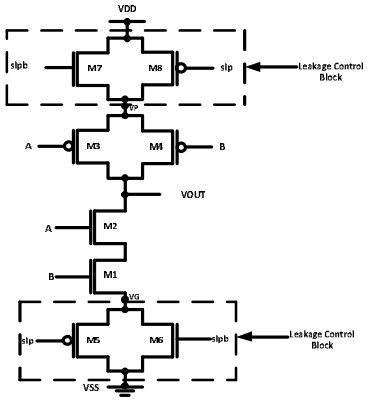

Fig. 9 LPSR NAND gate

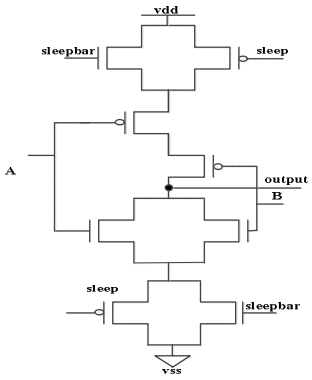

Fig. 10 LPSR NOR gate

A low leakage NAND and NOR gates with State Retention are shown in fig 9 and fig 10 respectively.

State retention novel low leakage NAND gate has four modes of operation:

a. Active mode: both sleep signals are used to switch on the leakage control transistors M5, M6, M7 and M8 by making slp=0 and slpb = 1. The node VG is at ground and the node VP is at VDD due to the presence of conventional sleep transistors M5and M6. The NAND gate thus sees good potential difference across nodes VP and VG and provides good output.

b. Deep Sleep mode: both sleep signals are used to switch off the leakage control transistors M5, M6, M7 and M8 by making slp=1 and slpb = 0. Thus the actual power and ground path are broken and the gate experiences lower voltage across the gates; a very high resistance path is established between VDD and ground and the leakage current flowing through the off transistors reduces significantly and hence reduced power dissipation.

c. State Retention with good 1: The sleep signals are maintained at slp=0 and slpb = 0, M5 and M8 are ON. The connection to ground is at VG and full VDD is provided. The state retention takes place with low leakage current due to off transistors M6 and M7.

d. State Retention with good 0: The sleep signals are maintained at slp = 1 and slpb = 1, M6 and M7 are ON.The connection to ground is complete and virtual VDD is provided. The state retention takes place and leakage current is lowered due to off transistors M5 and M8.

The states c and d activate one of the sleep control transistors M5 or M6 in the pull down path and M7 or M8 in the pull up path of gates and hence the state of the gates is preserved if there is no change in input value during standby mode of operation.

IV. SIMULATION AND RESULTS

All the logic gates discussed in this paper are designed using 90 nm CMOS process technology. The schematic design, simulation, functionality verification of these gates is performed using cadence virtuoso tool. The static power dissipation for all input combinations during all operating modes of logic gates and the total power consumption during pulsed operation are measured using cadence tools.

Table I provides Total power dissipation during pulsed operation for two input NAND and NOR gates. Table II provides comparison of the static power dissipation of all the NAND gates during active mode i.e. when sleep control signals slp and slpb hold the respective sleep transistors in the ON state and the gates behave in normal manner. This also provides static power dissipation during standby (sleep) mode of operation. Table III provides the static power dissipation during active and sleep mode of operation for all the NOR gates. For pulsed operation, transition period is taken as 2 us duration for all the circuits. All the gates are controlled by the sleep signals of same pulse width and period for the sake of comparison. Long sleep or inactive period is also introduced to observe the performance during sleep period. Depending upon whether PMOS or NMOS sleep transistor is driven slp and slpb assume logic states to make them ON or OFF. The logic values of these sleep signals for different modes of operation in case of different gates are provided in the tables of observation.

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TABLE I. TOTAL(AVERAGE) POWER DISSIPATION(IN WATTS) FOR 2 INPUT GATES

Gate	Total Power during Clocked Operation	Gate	Total Power during Clocked Operation
NAND	4.5340E-07	NOR	5.5610E-07
Sleepy NAND	4.6710E-09	Sleepy NOR	1.6170E-08
Sleepy Keeper NAND	2.6780E-08	Sleepy Keeper NOR	1.9340E-08
Power Gated NAND	4.6310E-08	Power Gated NOR	8.6020E-08
VCLEARIT NOR	3.8260E-08	VCLEARIT NOR	3.9820E-08
Ultra LP NAND	**6.7960E-12**	**Ultra LP NOR**	**1.0960E-08**
Data Retention NAND	**3.7772E-09**	**Data Retention NOR**	**1.3020E-08**

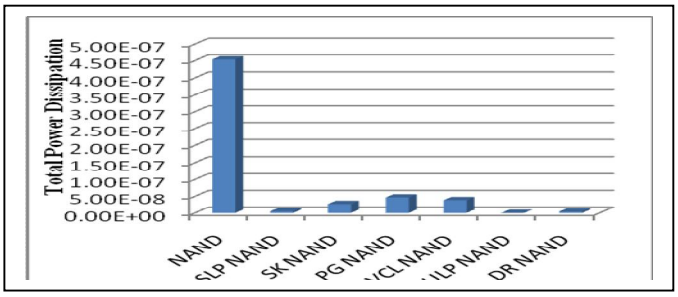
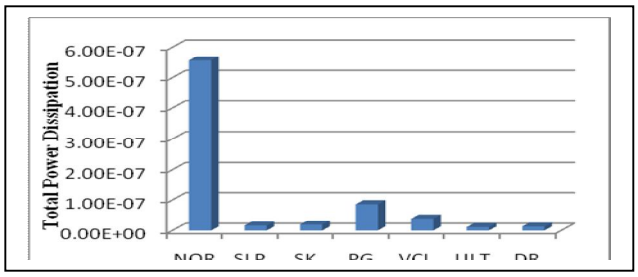


Fig. 11 Total Power Dissipation in different NAND Gates Gates



F ig. 12 Total Power Dissipation in different NOR

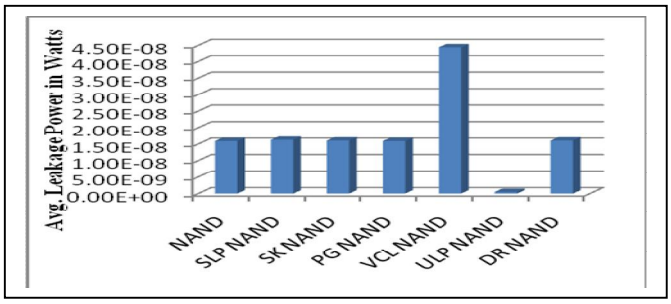


Fig.13 Active Mode Static Power Dissipation in different different NAND NAND Gates

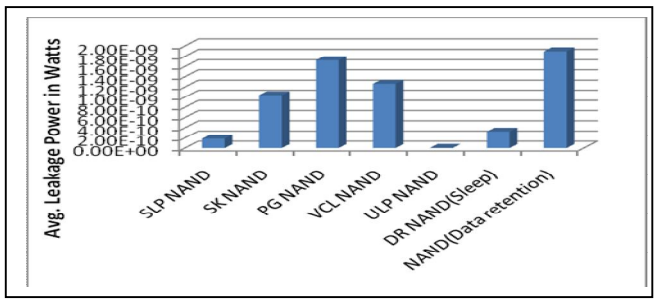


Fig. 14 Sleep Mode Static Power Dissipation in Gates

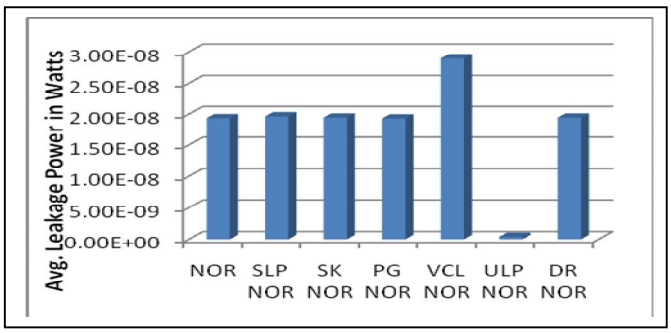


Fig. 15 Active Mode Static Power Dissipation in different different NOR NOR Gates

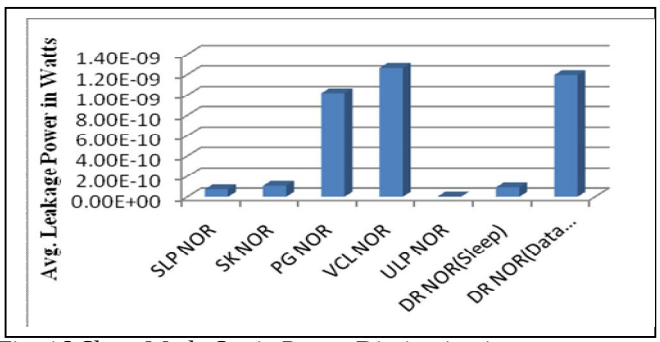


Fig. 16 Sleep Mode Static Power Dissipation in Gates

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TABLE II. STATIC POWER DISSIPATION FOR 2 INPUT NAND GATE

90 nm Technology with VDD = 1.1 Volt					
Gate	**Leakage power(in Watts) for input vectors in Active Mode**				**Avg. Leakage Power in Watts**
	0 0	**0 1**	**1 0**	**1 1**	
NAND	2.2070E-09	3.8012E-08	2.2524E-08	8.3128E-10	1.5894E-08
Sleepy NAND	2.6308E-09	3.8299E-08	2.2912E-08	1.2550E-09	1.6274E-08
Sleepy Keeper NAND	2.3770E-09	3.8115E-08	2.2686E-08	1.0025E-09	1.6045E-08
Power Gated NAND	2.2069E-09	3.7979E-08	2.2517E-08	8.3127E-10	1.5884E-08
VCLEARIT NAND	4.0335E-08	7.6071E-08	6.0634E-08	6.7230E-10	4.4428E-08
Ultra LP NAND(slp =0, slpb = 1)	**7.0273E-10**	**5.4362E-10**	**5.9676E-10**	**1.3091E-10**	**4.9351E-10**
Data Retention NAND(slp = 0, slpb = 1)	**2.3765E-09**	**3.8114E-08**	**2.2685E-08**	**1.0006E-09**	**1.6044E-08**
	Leakage power(in Watts) for input vectors in Sleep Mode				
NAND	NA				
Sleepy NAND	2.5032E-10	2.3861E-10	2.3646E-10	1.1307E-11	1.8417E-10
Sleepy Keeper NAND	9.7452E-10	1.4624E-09	1.7098E-09	7.2076E-12	1.0385E-09
Power Gated NAND	1.6701E-09	2.1735E-09	2.3440E-09	7.0884E-10	1.7241E-09
VCLEARIT NAND	1.6874E-09	1.2634E-09	1.2634E-09	8.3954E-10	1.2634E-09
Ultra LP NAND(slp = 1, slpb = 0)	7.0656E-12	3.2649E-12	9.0115E-13	4.7140E-13	2.9258E-12
Data Retention NAND(slp=1,slpb=0)(Sleep Mode)	**4.4316E-10**	**4.3479E-10**	**4.1266E-10**	**7.2329E-12**	**3.2446E-10**
Data Retention NAND(Slp=0,slpb=0)(Data Retention)	**1.8416E-09**	**2.3450E-09**	**2.5155E-09**	**8.8019E-10**	**1.8956E-09**

TABLE III. STATIC POWER DISSIPATION FOR 2 INPUT NOR GATE DURING ACTIVE MODE

90 nm Technology with VDD = 1.1 Volt					
Gate	**Leakage power(in Watts) for input vectors in Active Mode**				**Avg. Leakage Power in Watts**
	0 0	**0 1**	**1 0**	**1 1**	
NOR	7.6194E-08	8.3954E-10	2.4107E-10	1.0695E-11	1.9321E-08
Sleepy NOR	7.6079E-08	1.2634E-09	6.6491E-10	4.3459E-10	1.9610E-08
Sleepy Keeper NOR	7.6099E-08	1.0109E-09	4.1254E-10	1.8221E-10	1.9426E-08
Power Gated NOR	7.6064E-08	8.3954E-10	2.4107E-10	1.0686E-11	1.9289E-08
VCLEARIT NOR	1.1410E-07	8.8437E-10	4.4955E-10	2.5050E-10	2.8921E-08
Ultra LP NOR(slp = 0, slpb = 1)	**1.0289E-09**	**3.7604E-10**	**8.8694E-11**	**8.8802E-12**	**3.7563E-10**
Data Retention NOR(slp = 0, slpb = 1)	**7.6098E-08**	**1.0089E-09**	**4.1058E-10**	**1.8027E-10**	**1.9424E-08**
	Leakage power(in Watts) for input vectors in Sleep Mode				
NOR	NA				
Sleepy NOR	2.2379E-10	4.7784E-11	1.0349E-11	4.7243E-12	7.1662E-11
Sleepy Keeper NOR	3.7926E-10	3.1959E-11	6.6671E-12	4.4556E-12	1.0559E-10
Power Gated NOR	3.0130E-09	8.1454E-10	2.4021E-10	1.0619E-11	1.0196E-09
VCLEARIT NOR	1.6874E-09	1.2634E-09	1.2634E-09	8.3954E-10	1.2634E-09
Ultra LP NOR(slp = 1, slpb = 0)	7.0597E-12	3.8386E-12	6.2855E-13	4.5839E-13	2.9963E-12
Data Retention NOR(slp=1, slpb=0)(Sleep Mode)	**3.2029E-10**	**3.1974E-11**	**6.6819E-12**	**4.4920E-12**	**9.0859E-11**
Data Retention NOR(Slp=0, slpb=0)(Data Retention)	**3.2023E-09**	**9.8595E-10**	**4.1166E-10**	**1.8212E-10**	**1.1955E-09**

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V.CONCLUSION

The sleep gates using ultra low leak methodology have exhibited lowest leakage current and lowest power. However during active mode lower output voltage is observed at correct functionality. The sleepy keeper approach though maintains state during sleep at reduced levels, results in large power dissipation. The proposed LPSR state retention gates do provide good logic levels at reduced power during active mode of operation. The leakage power during sleep is also lower and state retention can also be achieved at good logic levels. The Total power dissipation is least. Since single VTH transistors are used in all the designs to achieve low power the novel techniques provide new choice to the designers of low power logic gates.

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