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A Low Power Binary to Excess-1 Code Converter Using GDI Technique

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ABSTRACT: In this work a binary to excess-1 code converter is achieved by using GDI technique for the faster acceleration of the final addition in a hybrid adder. It is applied to the faster column compression multiplication using a combination of two design techniques: partition of the partial products into two parts for independent parallel column compression and acceleration of the addition using hybrid adder. The performance of the proposed design is compared with CMOS technology by evaluating the delay, power and transistor count with 180nm process technologies on Tanner EDA tools. The results show the proposed design is significantly lower than CMOS technology.

KEYWORDS*:* GDI, CMOS, Hybrid adder, binary to excess-1 code converter.

I. INTRODUCTION

Code conversions are very essential in digital systems. Design of area and power efficient high speed data path logic systems are one of the most substantial areas of research in VLSI system design. In digital adders the speed of addition is limited by the time required to propagate a carry through the adder. The sum for each bit position in an elementary adder is generated sequentially only after the previous bit position has been summed and a carry propagated into the next position. The CSLA is used in many computational systems to elevate the problem of carry propagation delay. However the CSLA is not area efficient because it uses multiple pairs of RCA(ripple carry adder) to generate partial sum and carry by considering carry input(Cin=0, Cin=1), then final sum and carry are selected by multiplexers. The power and area of CSA can be reduced by using BEC-1 converter instead of RCA.

In order to achieve efficient low power VLSI circuits we are illustrating a method of designing a binary to Excess-1 code converter with GDI technique. A combinational circuit of adder with multiplexer, binary to excess-1 code converter and ripple carry adder is called a Hybrid adder. Here the binary to excess-1 converter has a complex layout using CMOS logic in terms of area, delay and power consumption. Hence an attempt has been made to develop a converter for low power consumption and less complexity. The rest of the paper is organized as follows: section II deals with the concept of GDI technique. In section III, the design of binary to ecess-1 code converter is discussed. Section IV emphasizes on simulation results and discussion. Session V draws conclusion.

II. BASIC GDI CONCEPT

The GDI method is based on the use of a simple cell as shown in “Fig.1”. At first glance, the basic cell reminds one of the standard CMOS inverter, but there are some important differences 1) The GDI cell contains three inputs: G (common gate input of nMOS and pMOS), P (input to the source/drain of pMOS), and N (input to the source/drain of nMOS). 2) Bulks of both nMOS and pMOS are connected to N or P (respectively), so it can be arbitrarily biased at contrast with a CMOS inverter.

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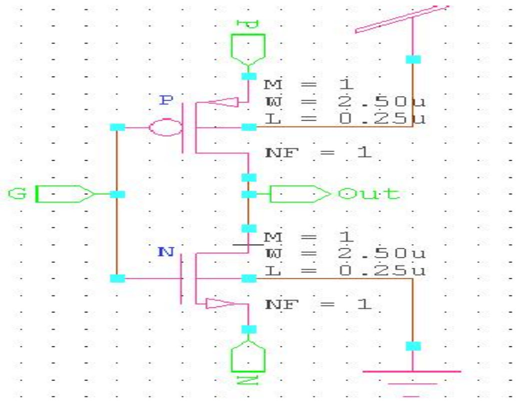

"Fig: 1". Basic GDI cell

Fig:1 represents the basic GDI cell (i.e.) inverter The GDI cell structure is different from the existing PTL techniques. It must be remarked that not all of the functions are possible in standard p-well CMOS process but can be successfully implemented in twin-well CMOS or silicon on insulator (SOI) technologies.

TABLE I

BASIC FUNCTIONS USING GDI CELL

N	P	G	OUTPUT	FUNCTION
0	1	A	A'	INVERTER
0	B	A	A'B	F1
B	1	A	A'+B	F2
1	B	A	A+B	OR
B	0	A	AB	AND
C	B	A	A'B+AC	MUX
B'	B	A	A'B+B'A	XOR
B	B'	A	AB+A'B'	XNOR

TABLE II

COMPARISON_OF_TRANSISTOR_COUNT_OF_GDI_AND STATIC_CMOS

FUNCTION	GDI	CMOS
INVERTER	2	2
F1	2	6
F2	2	6
OR	2	6
AND	2	6
MUX	2	12
XOR	4	16
XNOR	4	16
NAND	4	4
NOR	4	4

Table 1 describes the functions of basic gates. Table 2 shows the comparison between GDI and the static CMOS design in terms of transistors count. Any Boolean Function can be implemented using these universal gates.

III. DESIGN OF BINARY TO EXCESS-1 CONVERTER

A. Existing system

Code converters are very essential in digital systems. Here we are going to give the truth table for binary to excess-1 converter.Excess-1 converter is obtained by adding one to the binary value. The detailed structures of the 5-bit BEC without carry (BEC) and with carry (BECWC) are shown in “Fig.2”. The BEC gets *n* inputs and generates *n* output; the BECWC gets *n* input and generates *n+1* output to give the carry output as the selection input of the next stage *mux* used in the final adder design. The function table of BEC and BECWC are shown in Table III.

Table III
Truth table

Decimal Numerals	Binary numerals	Excess-1		
		Without carry	With carry	
			(carry)	
0	00000	00001	0	00001
1	00001	00010	0	00010
2	00010	00011	0	00011
3	00011	00100	0	00100
4	00100	00101	0	00101
5	00101	00110	0	00110
.	.	.	.	.
.	.	.	.	.
29	11101	11110	0	11110
30	11110	11111	0	11111
31	11111	00000	1	00000

Large bit sized multipliers requires multiple BEC and each of them requires the selection input from the carry output of the preceding BEC.

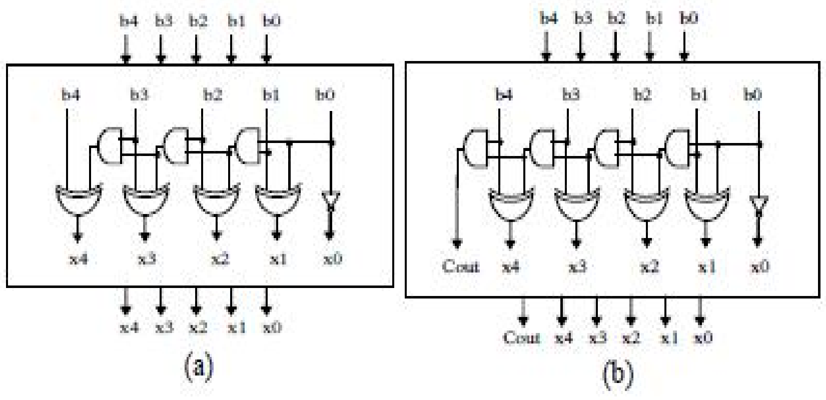

Figure. 2 The 5-bit Binary to Execss-1 Code Converter: (a) BEC (without carry), (b) BECWC (with carry).

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Therefore to generate the carry output from the BEC, an additional block is developed which is called BECWC (BEC With Carry). The detailed structures of the 5-bit BEC without carry (BEC) and with carry (BECWC) are shown “ Fig. 2(a) and Fig. 2(b)”.

B. Proposed system

It can be seen that large number of functions can be implemented using the basic GDI cell. Understanding of GDI cell properties demands a deeper operational analysis of the basic cell. Some of the digital circuits are implemented using 180nm CMOS process and the comparison is carried out between the standard CMOS logic and GDI Technique. In this proposed design the “Fig. 2(a) and Fig. 2(b)” were implemented using GDI. The following session describes the individual block representation of binary to excess-1 code converter.

1. Inverter

The design of GDI inverter using 180nm process is shown in “Fig.3”. 2 transistors are used in GDI as equal to CMOS.

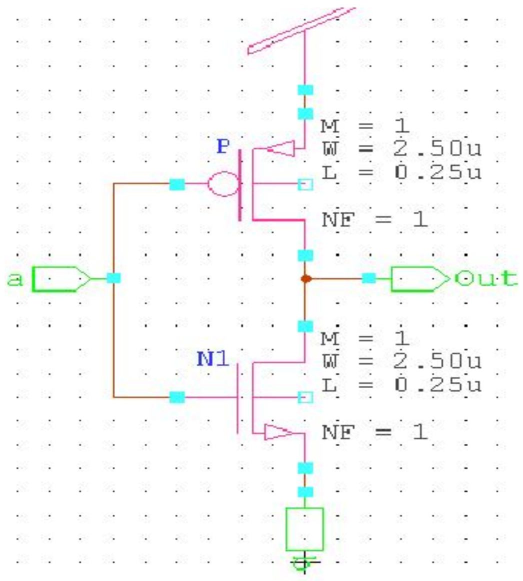

Fig.3 GDI inverter

2. AND gate

The AND gate is implemented in GDI using 180nm process technology. 2 transistors are used in GDI technique while 6 transistors in standard CMOS technology. The implementation is shown in “Fig.4”.

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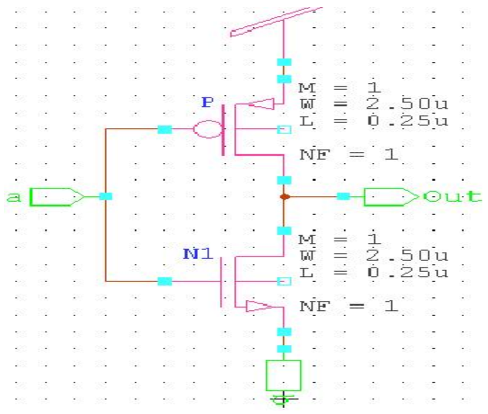

Fig.4 AND gate

3. XOR gate

XOR Gate is implemented using 180nm technology and the comparison is done among standard CMOS and GDI Techniques. Among the implemented techniques GDI consumes least power and the 4 transistors while 16 transistors using CMOS. The implementation is shown in “Fig. 5”.

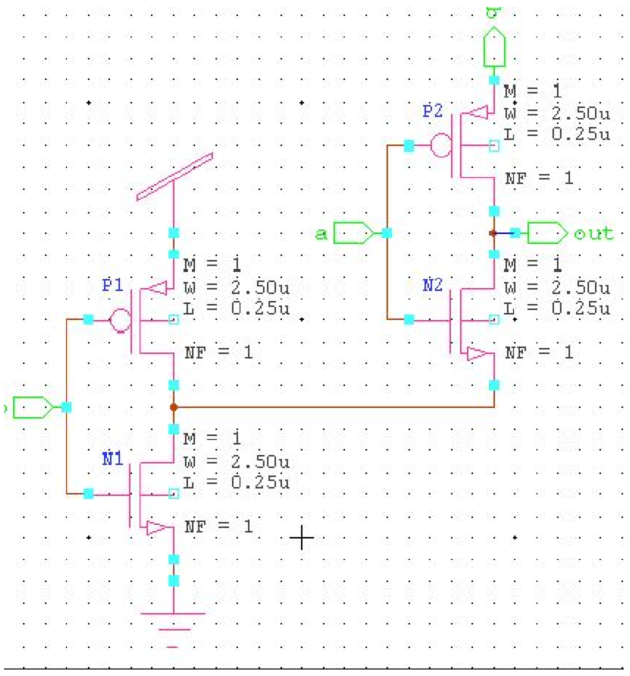

Fig.5 XOR gate

IV. RESULTS

The design is implemented using TANNER EDA tool. The performance comparison of binary to excess-1 converter using CMOS technology and GDI technique is given in Table IV and Table V.

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Table IV
BEC with carry

	Delay	Power consumption	Transistor count
CMOS	3.35	13.6 uw	90
GDI	3.06	11.2uw	26

Table V
BEC without carry

	Delay	Power consumption	Transistor count
CMOS	3.11	12uw	84
GDI	2.86	10uw	24

These are the outputs of basic GDI cell without employing any level restoring circuits at their outputs. The compared results summarize the enhanced performance of the proposed design for with carry and without carry are shown in Table IV and V. The power consumption of the proposed BEC for the 5-bit word size is 16% less when compared to CMOS. With increasing word size the difference in power requirement of the proposed BEC decreases. The delay values clearly indicate that the proposed BEC is 8% faster than the regular, also with increasing word size the percentage reduction of the delay increases.

V. CONCLUSION

A novel GDI technique for low power design was presented. Reduction of power in code converters has great importance in digital systems. The performance parameters like power, delay and transistor count are determined, analyzed, verified in GDI and compared with the existing CMOS technology.

VI. FUTURE SCOPE

Major application of BEC is to achieve faster acceleration of final addition in hybrid adder which is a combination of MBEC (MUX and BEC) and RCA (ripple carry adder). We hope the presented results will encourage further research activities on GDI technique.

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