

A Single-Phase Ac-Dc Converter with Improved Efficiency Using Atmega8 Microcontroller

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ABSTRACT: This paper proposed an AC-DC semi-bridgeless boost converter with 180 degree phase shift and less number of switches. The simplified current sensing method is applied in the converter to predict the inductor. The proposed converter has the advantageous features such as high efficiency at light loads and low ac input lines; compact in size, less charging time, and less amount and cost of electricity drawn. This project presented simulation results of a boost converter, converting the 230V ac input voltage to 400 V dc at upto 3kW Load. The power factor of the proposed system is maintained above 0.9 and the THD level is below 5%. The converter can works with less EMI. This type of converters is used for vehicle charging and residential charging application. The ATMEGA8 micro controller is for the controlling process, which has fast response with RISC architecture.

With solar source the semi bridgeless converter can acts as the dc-dc boost converter.

Keywords: AC-DC converter, boost converter, DC-DC converter, Bridgeless power factor correction (PFC), current sensing, plug in charger.

LINTRODUCTION

A storage system that can be recharged by connecting a plug to an external electric power source. The charging AC outlet predictably needs a plug in AC/DC charger with a power factor correction. For the PFC application a multiple of circuit topologies and control methods have been developed.

The single-phase active PFC techniques can be classified into two approaches: they are single-stage approach and the two-stage approach. The single-stage approach is right for low power level applications. It can only apply for lead acid batteries charging because of frequency ripple problem. Therefore, the two-stage approach is the most suitable for high storage battery chargers used for high power applications, where the power rating is relatively high, and lithium-ion batteries are used as the main energy storage system. In the two-stage architecture, the first stage is PFC rectification where it rectifies the input ac voltage and transfers it to a dc-link. At the same time, the PFC is also achieved. A phase shifted semi bridgeless PFC topology operated under continuous conduction mode as the two stage charger specifically with the ac-dc PFC converter and dc-dc converter for battery charging with various duty cycles.

A. Interleaved PFC boost topology

This boost topology uses two boost converters in parallel operating 180° out of phase [1]–[3] by switching 180° out of phase, it doubles the effective switching frequency and introduces a smaller input current ripple; thus, the input electromagnetic interference (EMI) filter can be smaller than a single PFC boost topology [4]–[6]. The drawback of this topology is the very high loss and the resultant heat management issue for the input diode bridge rectifiers.

B. Bridgeless PFC boost topology

This bridgeless boost topology avoids the need for the rectifier input bridge but maintains the classic boost topology [7]–[14]. The bridgeless boost converter, which is also called as the dual- boost PFC converter, which overcomes the problem of heat management in the input rectifier, diode bridge, but it introduces increased EMI [15]–[17]. The common-mode (CM) noise generated by bridgeless PFC is much higher than the conventional boost PFC

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topology [17]. The Drawback of this topology is the floating input line with respect to the PFC stage ground, which makes it impossible to sense the input voltage without a low-frequency transformer or an optical coupler.

C. Dual-boost PFC topology

The advantage of dual-boost PFC topology is [18] minimizes the gate loss, reduces the losses at light loads, the conduction loss can be minimized. The light-load efficiency, improved by an external device, which leads cost expense and improve controller complexity.

D. Semi-bridgeless PFC boost topology

Semi-bridgeless PFC boost topology is the conventional bridgeless topology with two extra slow diodes, that is, D_a and D_b that connect the input to the PFC ground. The slow diodes were added to address EMI-related issues [15],[16]. The current does not return through these diodes; therefore, their related conduction victims are small. The semi-bridgeless configuration also resolves the suspended input line problem with respect to the PFC stage ground.

E. Current sensing techniques

Three exclusive current-sensing circuits (Methods 1–3) for the bridgeless PFC boost topology are shown in Fig. 4 to sense the current in the MOSFET and diode paths independently, as the current path does not share the similar ground throughout each half-line cycle [7], [19].

Method 1 Fig. 1 (i) is the passive current-sensing scheme reported in [7], which requires three current-sensing transformers, one in series with each switch and a third in the positive dc rail to sense the collective current of the two diodes, and a supplementary signal transistor with its related difficult control circuitry.

Method 2 Fig.1 (ii) uses a simple, but the costly Hall Effect sensor to straightly sense the input current.

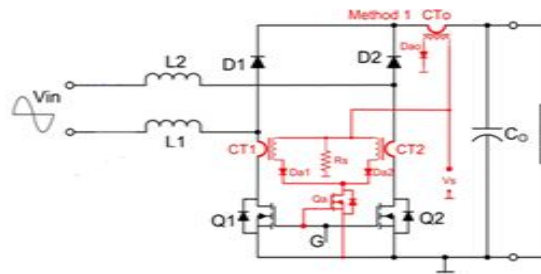


Fig. 1 (i). current-sensing method.1 implemented with bridgeless PFC topology.

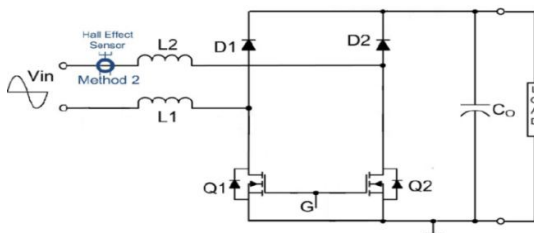


Fig 1(ii). current-sensing method.1 implemented with bridgeless PFC topology.

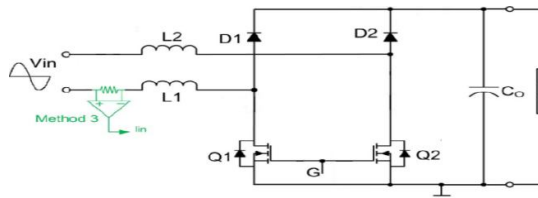


Fig 1(iii). current-sensing method.3 implemented with bridgeless PFC topology.

Method 3 Fig.1(iii). uses a differential-mode amplifier, which is connected in series with the input. This method is moderately less cost.

Where the current-sensing voltage is small to reduce the power loss, the power factor can be ruined by the sensing noise.

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II-PROPOSED SYSTEM

Vehicle storage charging is one of the applications of PSSB converter [22]. The Fig. 2. represents the block diagram of Phase Shifted boost power factor corrected converter.

PSSB BOOST CONVERTER

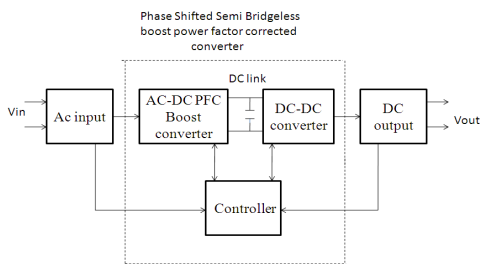


Fig.2. PSSB-block diagram

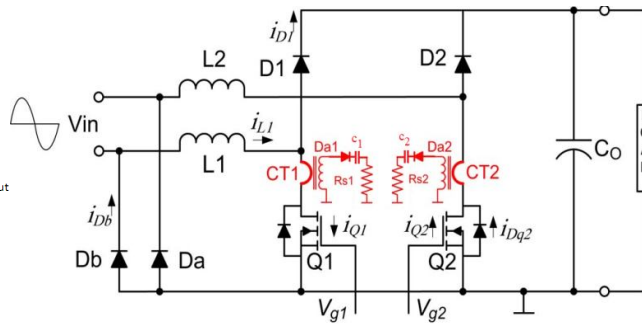


Fig. 3. Proposed PSSB PFC boost topology with the current-sensing circuit

The proposed PSSB topology shown in Fig.3. is used the current sensing method [20]. This method is used to find the inductor current by sensing the MOSFET current [21].

This topology consists the decoupled MOSFET gates, it uses two slow diodes (Da and Db), like to that of the semi-bridgeless PFC boost, to link the ground of the PFC to the input line. The gating signals for the MOSFETs are 180° out of phase. The proposed topology consists the advantages of both the bridge-less and semi-bridgeless boost PFC topologies. Its features are reduced EMI, high efficiency at light loads, and low lines, which is critical to minimize the charger size, cost, charging time, and amount and cost of electricity drawn.

The following section includes operation of the proposed converter and converter simulation output.

III-OPERATION OF CONVERTER

The proposed topology uses two slow diodes (Da and Db) to connect the ground of the PFC to the input line. The current does not return through these diodes, so their related conduction losses are low. The gating signals for MOSFETs are 180° out of phase. To evaluate the circuit operation, the input line cycle has been divided into the positive and negative half-cycles. The full circuit operation depends on the duty cycle.

A. POSITIVE HALF CYCLE OPERATION

During the positive half-cycle, when the input voltage is positive, Q1 turns on and current flows through L1 and Q1 and continues through Q2 and then L2, returning to the line while storing energy in L1 and L2. When Q1 turns off, energy stored in L1 and L2 is released as current flows through D1, through the load and returns through the body diode of Q2/partially through Db back to the input.

The detailed operation of the proposed converter depends on the duty cycle. During any half-cycle, the converter duty cycle is either greater than 0.5 (when the input voltage is smaller than half of output voltage) or smaller than 0.5 (when the input voltage is greater than half of output voltage).The following operating intervals are for which the duty cycle is less than 0.5.

Interval 1 [t0 – t1]: At t0, Q1/ Q2 are turned off,. During this interval, the energy stored in L1 and L2 is released to the output through L1, D1, partially Dq2, L2, and Db.

Interval 2 [t1 – t2]: At t1, Q1 is turned on, and Q2 is turned off,. During this interval, the current in series inductances L1 and L2 continues to increase linearly and store the energy in these inductors. The energy stored in Co provides energy to the load. The return current is split only between Db and Dq2.

Interval 3 [t2 – t3]: At t2, Q1/Q2 is turned off again, and interval 1 is repeated,. During this interval, the current in series inductances L1 and L2 decreases linearly, and the energy in these inductors is released. The energy stored in L1 and L2 is released to the output through L1, D1, partially Dq2, L2, and Db.

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Interval 4 [$t_3 - t_4$]: At t_3 , Q1 is off, and Q2 is turned on. During this interval, the energy stored in L1 and L2 is released to the output through L1, D1, partially Q2, Dq2, L2, and Db.

Detailed, Positive Half Cycle Operation and analysis for $D > 0.5$ and $D < 0.5$ is analyzed in [22].

B. NEGATIVE HALF CYCLE OPERATION

During the negative half-cycle, when the AC input voltage is negative, Q2 turns on and current flows through L2 and Q2 and continues through Q1 and then L1, returning to the line while storing energy in L2 and L1. When Q2 turns off, energy stored in L2 and L1 is released as current flows through D2, through the load and returns split between the body diode of Q1 and Da back to the input. The operation of converter during the negative input voltage half-cycle is similar to the operation of converter during the positive input voltage half-cycle.

IV-SIMULATION RESULTS OF PSSB BOOST SYSTEM

The Simulation of phase shifted semi bridgeless boost PFC converter is simulated for 1KW to 3KW load in MATLAB. Fig.4. shows the simulation and fig.5.gating signal for 180 degree phase shift.

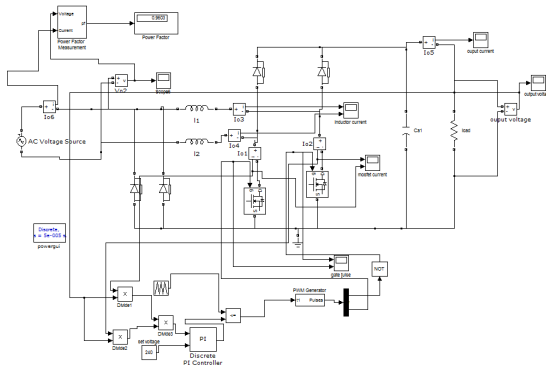


Fig.4.Simulation of Pssb

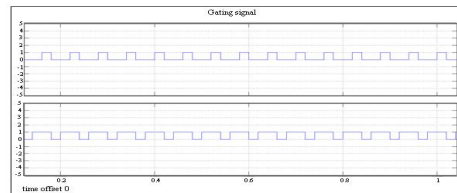


Fig.5.Gate signal waveform

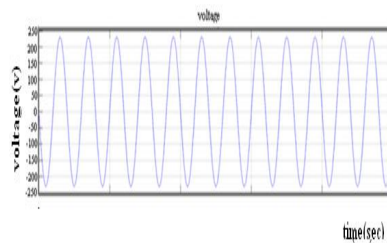


Fig.6. Input voltage

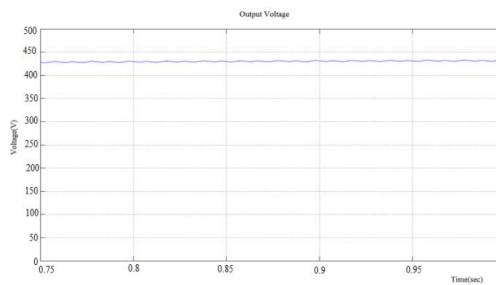


Fig.7. Output voltage

The Simulation results of input voltage and output voltage shown in fig.6.input voltage, fig.7. output voltage.

The THD value of proposed converter is below 5%.The fig.8. represents the output waveform of semi bridgeless converter with solar source. Here the converter is acts as the dc-dc converter when it is connected to solar panel. The maximum power point tracking is used to achieve the maximum amount of power.

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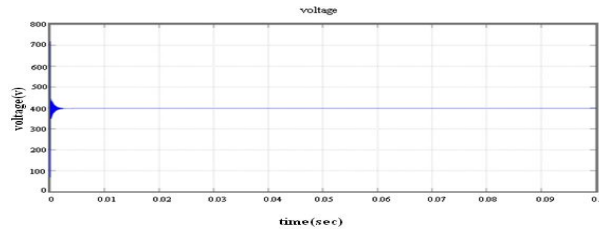


Fig.8. Output voltage

A.EXPERIMENTAL RESULT

As per simulation result the hardware can produce better results, which can able to boost up the input voltage. Components used in the hardware are specified in the below table.

COMPONENT NAME	RATINGS/PIN NUMBER	NO OF COMPONENTS
Inductor	1200 mH	2
Capacitor	1000 μ F	1
MOSFET	IRF 840	2
Diode	10A01	6
Current Transformer	0-5V,0-10A	2
Resistor	10K Ω	2

Controller: ATMEGA8 microcontroller

Table.1.List of components

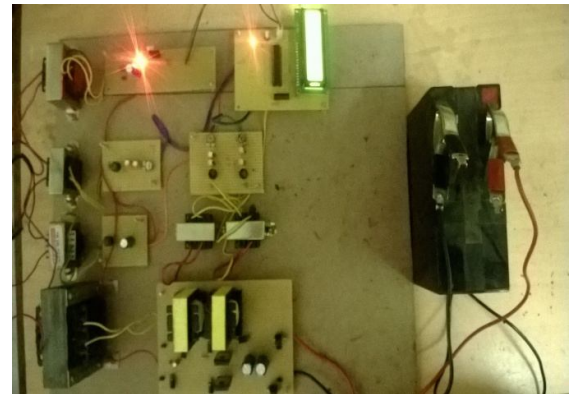


Fig.9.Hardware system

V-CONCLUSION

A better-performance Phase Shifted Semi Bridgeless boost converter topology has been proposed with the current sensing method. The converter advantageous features are high efficiency at light-load and low-line conditions, small in charger size, less cost, less charging time, and less cost of electricity. The input supply of the converter is 230V. While using this proposed converter system current THD is less than 5% for 1KW to 3KW load. The power factor is greater than 0.9 from 50% load to full load. It can provide better out voltage while it acts as the dc-dc converter.

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- Figure.3 is taken from ref.22.