ISSN (Print) : 2320 – 9798
ISSN (Online): 2320 – 9801

International Journal of Innovative Research in Computer and Communication Engineering
Vol. 1, Issue 4, June 2013

METAPHORICAL STUDY OF REVERSIBLE LOGIC GATES

Shweta Agrawal

M Tech [VLSI], Shri Ram College of Engineering and Management, Gwalior, India

Abstract: In today's world power dissipation is the main problem in digital world; this problem can be reduced by using reversible logic gates. For high performance systems, low power and smaller area are the most important criteria. Area and speed are main factors which are conflicting i.e. if speed is improving it results in larger area, hence in this paper reversible logic gates are analyzed. The power dissipation by these gates is very low; ideally their internal power dissipation is zero because these gates do not loss information. Systems where low power dissipation is required reversible logic gates will be used in place of classical logical gates like AND, OR, NAND, NOR. Reversible logic provides an alternative that may overcome many of these problems in the future.

By reducing the number of reversible logic gates one can minimize the quantum cost of these gates. Reversible logic finds its application in low power CMOS, quantum computing, nanotechnology, bio-information etc

Keywords: Reversible logic, Reversible logic gate, quantum computing, nanotechnology.

I. INTRODUCTION

The main aim of VLSI Circuit Design is very low power dissipation and improves system performance. According to R.Landauer researcher there is power dissipation of KTln2 joules of heat energy per bit of information loss in classical gates, where K is Boltzmann's constant and T the absolute temperature at which circuit performs [1].

Reversible logic does not loss any information. Reversible logic gate are the device which has n×n inputs and outputs, its means input is equal to output or there is one to one mapping. Any gate is said to be reversible if the input can be recovered from the output.

A Reversible circuit has the facility to generate a unique output vector from each input vector, and vice versa.

Input Vector

$I_v=(I_{i,j} , I_{i+1,j} , I_{i+2,j} , \quad \dots \quad , I_{k-1,j}, I_{k,j})$

Output Vector

$O_v=(O_{i,j} , O_{i+1,j} , O_{i+2,j} , \quad \dots \quad , O_{k-1,j}, O_{k,j})$

For each particular vector j

$I_v \leftrightarrow O_v$

Reversible are circuits in which the number of inputs is equal to the number of outputs and there is one-to-one mapping between vectors of inputs and outputs.

Difference between Reversible Gate and Irreversible Gate

A	B	Y
0	0	0
0	1	1
1	0	1
1	1	0

Table 1: Truth Table for Irreversible EXOR Logic

A	B	P	Q
0	0	0	0
0	1	0	1
1	0	1	1
1	1	1	0

Table 2: Truth Table for reversible EXOR Logic

ISSN (Print) : 2320 – 9798
ISSN (Online): 2320 – 9801

International Journal of Innovative Research in Computer and Communication Engineering
Vol. 1, Issue 4, June 2013

Features of reversible logic:
1. One to one mapping i.e. equal no of input and output.
2. For each input there is different output.
3. Fan out is not allowed.

Features of reversible logic circuit [6]:
1. Minimum number of reversible gates is used.
2. Minimum number of constant inputs is used.
3. Minimum number of garbage outputs should be there.
4. The length of cascading gates is minimum.

Basic Reversible logic Gates:

- N= No. Of reversible logical gate used in circuit.
- CI= No. of inputs that are at constant 0 or 1 for synthesis of any given logical functions.
- GO= No. of unused outputs in reversible logic.

II. TYPES OF REVERSIBLE LOGIC GATES

1. **Feynman Gate***:* It is a 2×2 reversible gate. A, B is input vector and P, Q is output vector. The output P=A, Q=A⊕B. It is used where copying is required and inverter both at the same time due to its output. The block diagram of this gate is shown in Fig .1

Figure .1 Block diagram of Feynman Gate

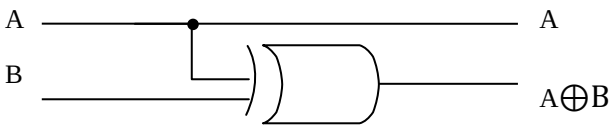

Figure.2 Combinational Circuit of Feynman gate.

A	B	P	Q
0	0	0	0
0	1	0	1
1	0	1	1
1	1	1	0

Table 3: Truth Table of Feynman gate

2. **Double Feynman Gate (F2G)**: It is 3×3 Double Feynman gate. A, B, C are input vector and P, Q, R are output vector, where P = A, Q=A⊕B and R=A⊕C. The block diagram of this gate is shown in Fig.3

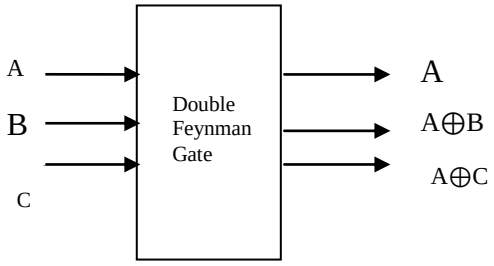

Figure .3 Block diagram of Double Feynman Gate

ISSN (Print) : 2320 – 9798
ISSN (Online): 2320 – 9801

International Journal of Innovative Research in Computer and Communication Engineering
Vol. 1, Issue 4, June 2013

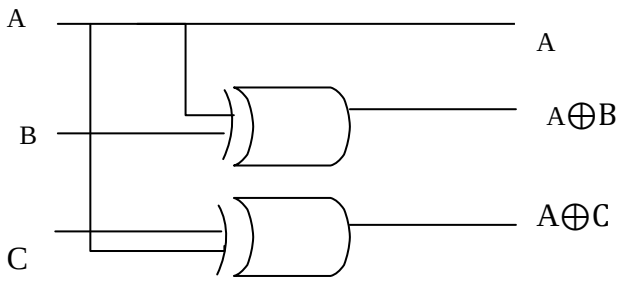

Figure.4 Combinational Circuit of Double Feynman gate

A	B	C	P	Q	R
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	0
0	1	1	0	1	1
1	0	0	1	1	1
1	0	1	1	1	0
1	1	0	1	0	0
1	1	1	1	0	0

Table 4: Truth table of Double Feynman Gate.

3. **Toffoli Gate**: It is 3×3 reversible logic gate having A,B,C as input vector and P,Q ,R as output vector, where P=A,Q=B and R=AB ⊕ C The block diagram of this gate is shown in Fig.5

Figure.5 Block diagram of Toffoli Gate

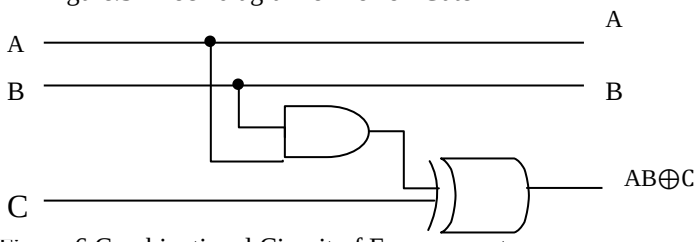

Figure.6 Combinational Circuit of Feynman gate

A	B	C	P	Q	R
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	0
0	1	1	0	1	1
1	0	0	1	0	0
1	0	1	1	0	1
1	1	0	1	1	1
1	1	1	1	1	0

Table 5: Truth Table of Toffili Gate

ISSN (Print) : 2320 – 9798
ISSN (Online): 2320 – 9801

International Journal of Innovative Research in Computer and Communication Engineering
Vol. 1, Issue 4, June 2013

4. **Fredkin Gate :**It is 3×3 reversible logic gate having A,B,C as input vector and P,Q,R as output vector, where P=A,Q=A'B⊕AC , R=A'C⊕AB The block diagram of this gate is shown in Fig.8

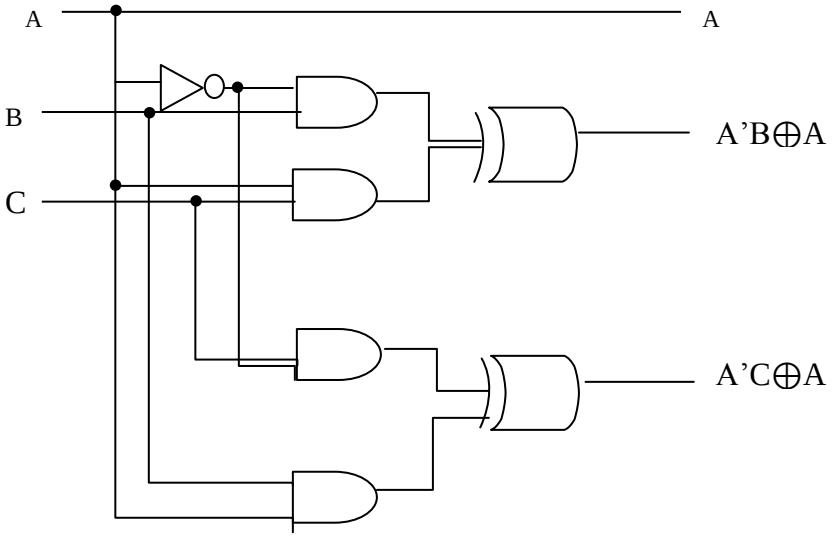

Figure.7 Combinational Circuit of Fredkin gate

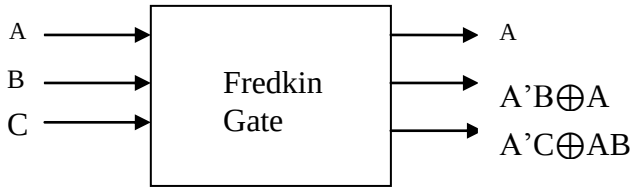

Figure.8 Block diagram of Fredkin gate

A	B	C	P	Q	R
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	0
0	1	1	0	1	1
1	0	0	1	0	0
1	0	1	1	1	0
1	1	0	1	0	0
1	1	1	1	1	1

Table 6: Truth Table of Fredkin Gate

5. **Peres Gate**: It is 3×3 reversible logic gate. A, B, C is input vector and P, Q, R is output vector, where P = A, Q = A⊕B and R=AB⊕ C. The block diagram of this gate is shown in Fig.9

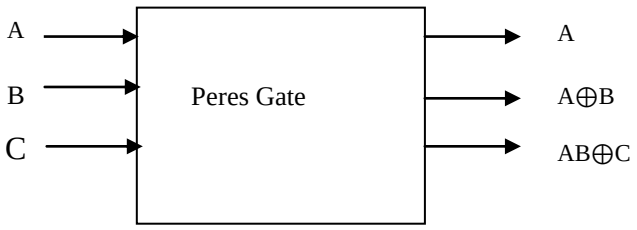

Figure.9 Block diagram of Peres gate

ISSN (Print) : 2320 – 9798
ISSN (Online): 2320 – 9801

International Journal of Innovative Research in Computer and Communication Engineering
Vol. 1, Issue 4, June 2013

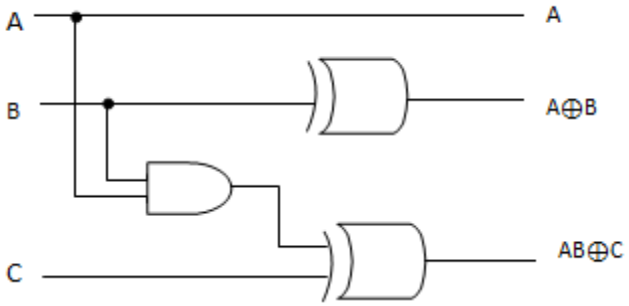

Figure.10 Combinational Circuit of Peres gate

A	B	C	P	Q	R
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	0
0	1	1	0	1	1
1	0	0	1	1	0
1	0	1	1	1	1
1	1	0	1	0	0
1	1	1	1	1	0

Table 7: Truth Table of Peres Gate

6. **TSG gate**: It is 4×4 reversible gate. A, B, C, D is input vector and P, Q, R, S is output vector, output P = A, Q = A'C'⊕B', R = (A'C'⊕B') ⊕ D and S = (A'C'⊕B').D⊕ (AB⊕C), the block diagram of this gate is shown in Fig.11

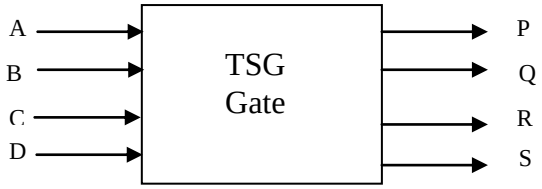

Figure.11 Block diagram of TSG gate

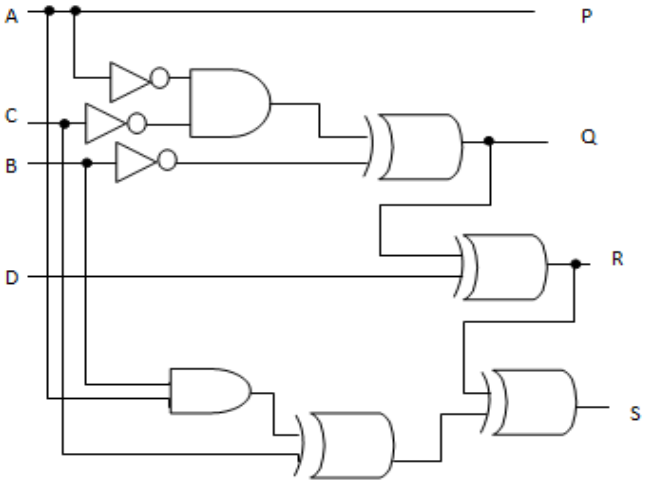

Figure.12 Combinational Circuit of Peres gate

ISSN (Print) : 2320 – 9798
ISSN (Online): 2320 – 9801

International Journal of Innovative Research in Computer and Communication Engineering
Vol. 1, Issue 4, June 2013

A	B	C	D	P	Q	R	S
0	0	0	0	0	0	0	0
0	0	0	1	0	0	1	0
0	0	1	0	0	1	1	1
0	0	1	1	0	1	0	1
0	1	0	0	0	1	1	0
0	1	0	1	0	1	0	0
0	1	1	0	0	0	0	1
0	1	1	1	0	0	1	1
1	0	0	0	1	1	1	0
1	0	0	1	1	1	0	0
1	0	1	0	1	1	1	1
1	0	1	1	1	1	0	1
1	1	0	0	1	0	0	1
1	1	0	1	1	0	1	1
1	1	1	0	1	0	0	0
1	1	1	1	1	0	1	0

Table 8: Truth table of TSG Gate

7. **Sayem gate**: It is 4×4 reversible gate. A, B, C, D is input P, Q, R, S is output vector, where P=A, Q=A'B⊕ AC, R= A'B ⊕AC⊕ D, S=AB ⊕A'C ⊕ D). The block diagram of this gate is shown in Fig.13

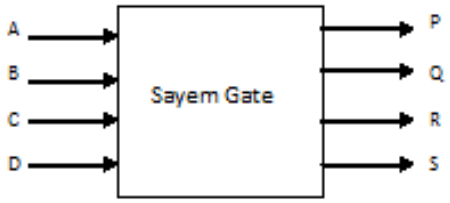

Figure.13 Block diagram of Sayem gate

A	B	C	D	P	Q	R	S
0	0	0	0	0	0	0	0
0	0	0	1	0	0	1	1
0	0	1	0	0	0	0	1
0	0	1	1	0	0	1	0
0	1	0	0	0	1	1	0
0	1	0	1	0	1	0	1
0	1	1	0	0	1	1	1
0	1	1	1	0	1	0	0
1	0	0	0	1	0	0	0
1	0	0	1	1	0	1	1
1	0	1	0	1	1	1	0
1	0	1	1	1	1	0	1
1	1	0	0	1	0	0	1
1	1	0	1	1	0	1	0
1	1	1	0	1	1	1	1
1	1	1	1	1	1	0	0

Table 9: Truth table of Sayem Gate

ISSN (Print) : 2320 – 9798
ISSN (Online): 2320 – 9801

International Journal of Innovative Research in Computer and Communication Engineering
Vol. 1, Issue 4, June 2013

III. APPLICATIONS

Reversible logic finds its application in computer security and transaction processing, as it possess high energy efficiency, speed and performance.

IV. CONCLUSION

The paper reveals that reversible logic gates outperform classical logic gates. The prospect for further research includes quantum computing and Nano technology.

ACKNOWLEDGMENT

We take this opportunity to express our deepest gratitude and appreciation to all those who have helped us directly or indirectly towards the successful completion of this paper.

REFERENCES

[1] R. Landauer, "Irreversibility and Heat Generation in the Computational Process" IBM Journal of Research and Development, vol.5, pp. 183-191, 1961.

[2] Bennett, C.H., "Logical reversibility of Computation", IBM Journal of Research and Development, vol.17, pp. 525-532, 1973.

[3] Mr. Devendra Goyal, "VHDL Implementation of Reversible Logic Gates" International Journal of Advanced Technology & Engineering Research (IJATER), Vol. 2, Issue 3, May 2012.

[4] Feynman, "Quantum mechanical computers", Optics News, pp. 11-20, 1985.

[5] Toffoli.T, "Reversible Computing", Tech memo MIT/LCS/TM-151, MIT lab for Computer Science, 1980.

[6] Vasudevan.D.P , Lala.P.K and Parkesson.J.P, "Online Testable Reversible Logic circuit Design using NAND Blocks", Proc. Symposium on Defect and *Fault Tolerance*, pp. 324-331, 2004.

[7] E. fredkin, T. Toffoli, "Conservative Logic", International Journal of Theory of Physics, vol.21, pp 219-253,1982.

[8] Md. M.h. Azad Khan, "design of full-adder with reversible gates" International conference on computer & information technology. Dhaka, Bangladesh, pp.515-519, 2002

[9] Bhagyalakshmi, H.R. ;.Venkatesha, M.K, "An improved design of a multiplier using reversible logic gates", International Journal of Engineering Science and Technology Vol. 2,pp. 3838-3845,2010.

[10] Michael P. Frank ," Reversibility for efficient computing", Ph. D. Thesis, May 1999.

[11] Carlin Vieri "Reversible Computing for Energy Efficient and Trustable computation", April 1998.