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Wideband Variable Gain Amplifier in 0.13µm CMOS Technology

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ABSTRACT: Synthetic Aperture Radar (SAR) is a well known technique for imaging the earth's surface. This paper presents a wideband variable gain amplifier (VGA) which can be used in the direct conversion receiver (DCR) for SAR. This paper first introduces how to extract the important parameters i.e. gain, bandwidth and power consumption of the VGA from the overall receiver requirements. VGA has designed for 2.4GHz Bandwidth and simulations are done using 0.13um technology level-54 model files on HSPICE Simulator. The proposed VGA circuit has a variable gain of (4.43 – 15.14) dB and -3dB frequency falls at 2.398GHz. The power consumption is only 1.803mW and the supply voltage is about 1.8v.

KEYWORDS: CMOS,Wideband, variable gain amplifier, low power consumption, differential amplifier.

I.INTRODUCTION

Synthetic Aperture Radar (SAR) is a well known technique for imaging the earth's surface. Some of its most important applications include disaster management, land and sea traffic observation, wide area surveillance, and environmental monitoring. SAR systems use radar signals and complex electronics to provide broad-area imaging capability. The most attractive feature of SAR systems is their ability to provide day-and-night imagery of earth, independent of weather conditions [1]. In order to overcome the limitation of imaging wide swath, with simultaneously high resolution, SAR systems employ receiving antenna with multiple sub-apertures, each sub aperture with its own independent receiver [2]. Each of the *N* sub apertures on the receive antenna has its own receiver. The digitized signals from each of these receivers can then be stored and digitallyprocessed a posterioris to form a high resolution image of a large area. In such a system it would be beneficial to realize each of the independent receivers with highly integrated CMOS circuits that have small silicon footprint andoverall low power consumption. The direct conversion receiver (DCR) which down converts the RF signal directly to its base band. DCR has the advantage that it requires no off-chip image reject filters. Moreover, it only requires low-pass filters and amplifiers that are amenable to monolithic integration. In this journal, the design of a wideband variable gain amplifier (VGA) is described which is to be used in the DCR for SAR systems. Therefore small silicon area and low power consumption are the basic goals for the design.

II. LETERATURE SURVEY

FilipTavernier and MichielSteyaert,proposed "A low power limiting amplifier with area efficientoffset compensation in 90nm CMOS". The largetime constant needed in the offset compensation feedback loop isboosted by an inverting amplifier to reduce the chip area [3]. On topof this, to reduce the chip area even more, negative capacitors areapplied to increase the bandwidth instead of making use of theinductive peaking technique. The proposed circuit has a small-signalgain of 35dB and a bandwidth of 4.15GHz. The power consumption is having only 14.7mW.

Ville Saari,MikkoKaltiokallio, SaskaLindfors,JussiRyynänenandKari A.I.Halonen,proposed"A 240-MHz Low-Pass Filter With Variable Gain in65-nm CMOS for a UWB Radio Receiver" An integrated fifth-order continuous-time low-passfilter for a WiMedia ultrawideband radio receiver is described inthis paper [6]. The passbandedge frequency of the implemented filter is 240 MHz in order toreceive multiband-orthogonal-frequency-division-multiplexingsignals using the direct-conversion topology. The voltage gain ofthe filter can be controlled from 9 to 43 dB in the 1-dB gain steps. The circuit uses a 1.2V supply.

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YuanjinZheng, Jiangnan Yan, and Yong Ping Xu, proposed "A CMOS VGA With DC Offset Cancellation forDirect-Conversion Receivers"A CMOS dB-linear variable gain amplifier (VGA)with a novel I/Q tuning loop for dc-offset cancellation is presented.The CMOS dB-linear VGA provides a variable gain of 60 dB whilemaintaining its 3-dB bandwidth greater than 2.5MHz. A novelexponential circuit is proposed to obtain the dB-linear gain controlcharacteristics. Nonideal effects on dB linearity are analyzed andthe methods for improvement are suggested. A varying-bandwidthLPF is employed to achieve fast settling. The chip is fabricated in a 0.35µm CMOS technology.

Quoc-Hoang Duong, Chang-Wan Kim, and Sang-Gug Lee,proposed"A 95-dB Linear Low-Power Variable Gain Amplifier" this paper [8], designs the variable gain amplifier in 180nm CMOS technology uses the supply voltage of 1.8v and the variable gain of (47.5 - 95)dB. The -3dB frequency of 32MHz and having the power consumption is only 6.7mW.

III. VARIABLE GAIN AMPLIFIER (VGA)

A. STAGE-1 VGA:

The first stage of the VGA should be a high-gain, low-noise stage. Moreover the -3 dB bandwidth of this stage has to be much higher than the overall bandwidth of the VGA. Based on these requirements, a active loaded source-coupled differential pair was chosen. The schematic of the circuit is shown is Fig.1M_{1a} and M_{1b} form the source-coupled pair with active loads $M_{2a}$and M_{2b}. The I_1 acts as a tail current source. Resistor R_{g1} represents the resistance of the driving source. That the Miller effect increases the input capacitance and the pole formed by R_{g1} and the total input capacitance of the stage limit the -3 dB bandwidth of the amplifier. In order to suppress the Miller-effect and increase the bandwidth of the stage, negative Miller capacitors (C_{c1a} and C_{c1b}) have been used. These capacitors were chosen to push the input pole to higher frequency. C_{L1} represents the capacitive loading at the output V_{OUT1}. It includes the intrinsic capacitance of the transistor *M1b*, the wiring capacitance and the input capacitance of the next stage.

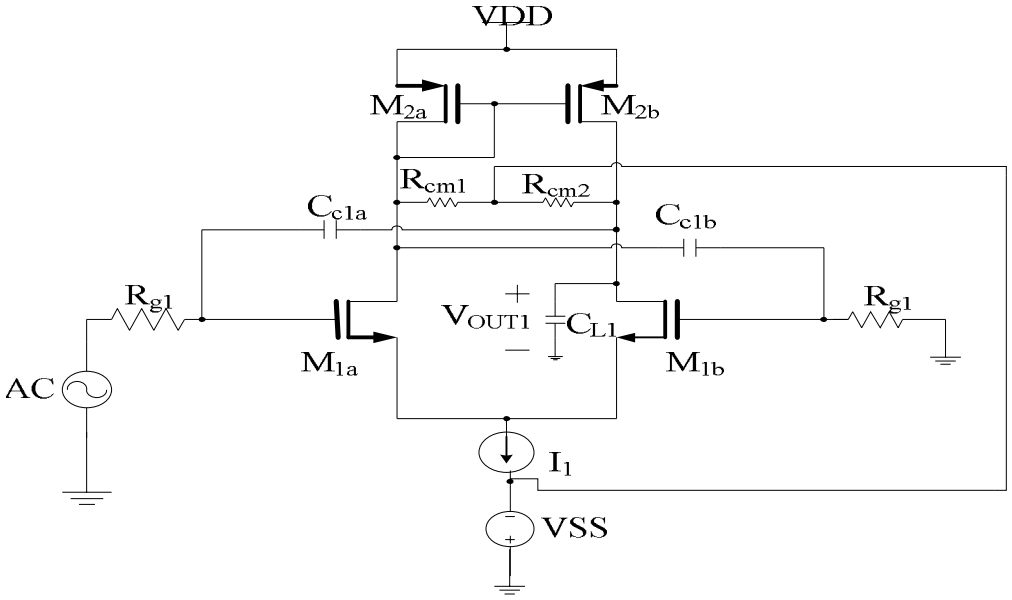

Fig.1 Schematic of VGA Stage-1

Due to the balanced structure of stage-1 VGA, only the half-circuit analysis can be used in the equivalent small-signal model. Since negative miller capacitors ($C_{c1a}$and C_{c1b}) cancel out the gate-drain capacitance C_{gd} of the transistor M_{1a} and $M_{1b,}$ theyhave been ignored in the equivalent small-signal circuit. The small-signal voltage v_{out1}can be expressed as$v_{out1}(s) = -g_{m1a}v_{gs1}(s)(r_{01a} \| r_{02a} \| \frac{1}{sC_{L1}})$,

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Where r_{01a} and r_{02a} are the output resistance of the transistors M_{1a} and M_{2a}. v_{out1} can be written as

$$v_{out1}(s) = -g_{m1a}v_{gs1}(s)((r_{01a}\|r_{02a})\|\frac{1}{sC_{L1}}),$$

$$v_{out1}(s) = -g_{m1a}v_{gs1}(s)\left[\frac{(r_{01a}\|r_{02a})}{1+s(r_{01a}\|r_{02a})C_{L1}}\right], \quad (1)$$

The DC voltage gain of stage-1 A_{v1} is given as

$$A_{v1} = -g_{m1a}(r_{01a}\|r_{02a}) \quad (2)$$

From eq.4.1.1 the poles *P1* and *P2* are obtained as

$$P1 = \frac{1}{(r_{01a}\|r_{02a})C_{L1}} \text{ , and} \quad (3)$$

$$P2 = \frac{1}{R_{g1}C_{gs1a}}. \quad (4)$$

Notice that typically P_1 forms the dominant pole because $C_{L1} > Cgs1a$. Also for high gain r_{02a} should be increased but for high bandwidth r_{02a} should be decreased. Thus there is an optimum value of r_{02a} that will satisfy both the gain and bandwidth requirements and in the VGA design, Simulations (using HSPICE) was used to determine it.

B. STAGE-2 & 3 VGA:

It has already been shown that using two stages in the variable gain section of the amplifier gives the best gain-bandwidth product. For this purpose, a capacitive degenerated source-coupled differential pair is used in these stages. The schematic of the circuit is shown is Fig.2. M_{3a} and M_{3b} form the source-coupled pair with active loads M_{4a} and M_{4b}. R_S and C_S are the degeneration resistor and capacitor. The source I_2 and I_3 acts as tail current sources. Since stage-2 will be DC coupled with stage-1. Resistor *R*g2 represents the resistance of the driving source (in the full integrated VGA it will be the output resistance of the stage-1). Just like stage-1, Negative Miller capacitors (C_{c2a} and C_{c2b}) are used to suppress the Miller-Capacitance. C_{L2} is the capacitive loading at the output V_{OUT2}. It includes the intrinsic capacitance of the transistor M_{2b}, the wiring capacitance and the input capacitance of the next stage. The transfer function of the Stage-2&3 VGA is given by

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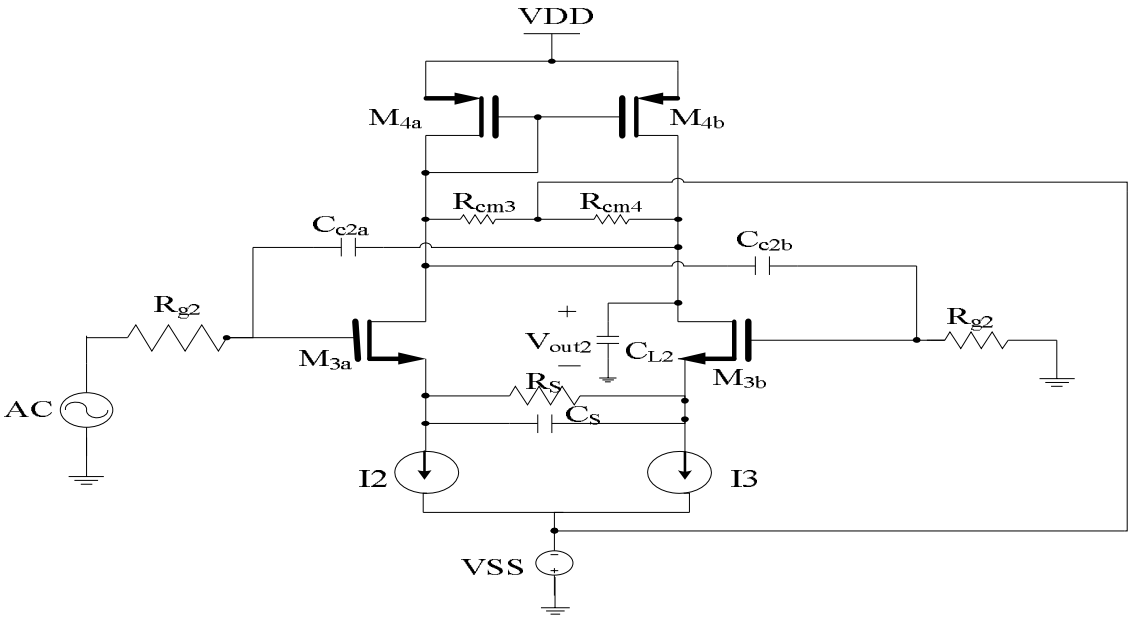

Fig.2

Schematic of VGA Stage-2 & Stage-3

$$\frac{v_{out2}(s)}{v_{in2}(s)} = \left[\frac{-g_{m3a}(r_{03a}\|r_{04a})}{s(r_{03a}\|r_{04a})C_{L2}+1}\right]\left[\frac{sR_sC_s+1}{s^2R_sC_sR_{g2}C_{gs2a}+s(R_sC_s+R_{g2}C_{gs2a}+0.5R_sC_{gs2a})+(1+0.5R_sg_{m3a})}\right] \quad (5)$$

From the Equation.5 the voltage gain of Stage-2&3 VGA , poles and zeros can be calculated as below

$$A_{v2} = -\frac{g_{m3a}(r_{03a}\|r_{04a})}{1+0.5R_sg_{m3a}}, \quad (6) z_1 = \frac{1}{R_sC_s} \quad (7)$$

$$P_1 = \frac{1}{(r_{03a}\|r_{04a})C_{L2}} \quad (8)$$

$$P_2 = \frac{1+0.5R_sg_{m3a}}{R_sC_s+R_{g2}C_{gs2a}+0.5R_sC_{gs2a}} \quad (9)$$

$$P_3 = \left[\frac{1}{R_sC_s}+\frac{1}{R_{g2}C_{gs2a}}+\frac{1}{2R_{g2}C_s}\right]. \quad (10)$$

IV. SIMULATION RESULTS

A. STAGE-1 VGA:

The stage-1 VGA has designed for the 2.344 GHz having the design specifications i.e. considering the $I_D = 1mA$so that the all the MOSFETS operate in 500uA current. The size of the NMOS is $(\frac{W}{L})_n = \frac{3495}{130}nm$ and the size of the PMOS is $(\frac{W}{L})_p = \frac{4190}{130}nm$. The Negative Miller Capacitors (C_{c1a} and C_{c1b}) are chosen to be 0.01pF in order to reduce the Miller Effect so that we can achieve wider bandwidth that can be used at Synthetic Aperture Radar (SAR) in Direct Conversion Receiver (DCR) for imaging the earth's surface. The common mode resistors (R_{CM1} and R_{CM2}) are chosen 1MΩ each for the proper gain correction. Fig.3 shows the gain of stage-1 versus the frequency. Note that the low-frequency gain is about 15.38 dB. And because of $C_{L1} = 0.017pF$ the -3 dB bandwidth achieved more than

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2.344GHz hence *P1* becomes the dominant pole since $C_{L1} > C_{gs1a}$. And power consumed in the circuit is 1.803mW. The Table.1 gives the performance comparison of present work with reference papers.

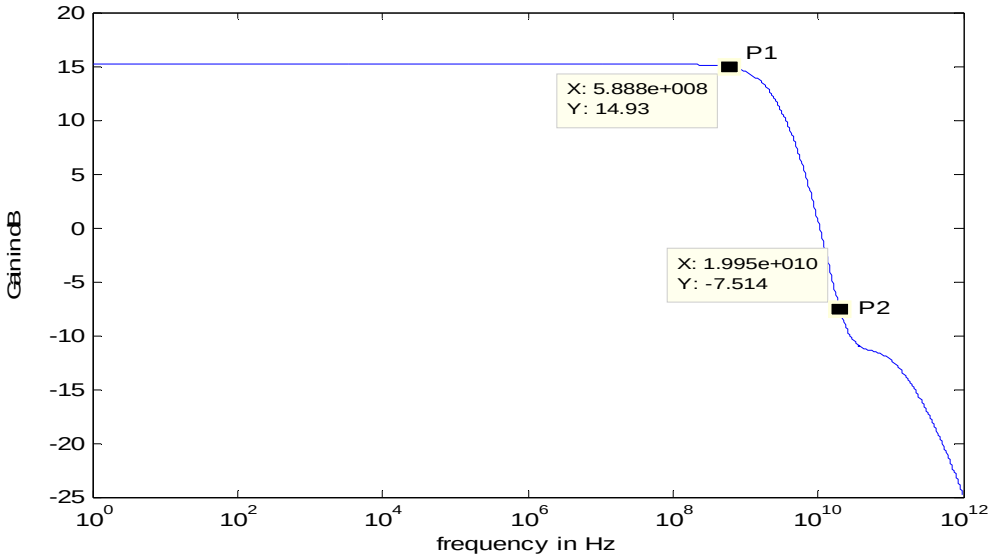

Fig.3 Gain (dB) of stage-1 of VGA versus frequency (Hz).

Parameters	[3]	[6]	[7]	[8]	**This work**
CMOS Technology	90nm	65nm	135nm	180nm	**130nm**
Supply Voltage	1v	1.2v	1.2v	1.8v	**1.8v**
Gain(dB)	35dB	(9-43)dB	(0-60)dB	(47.5 - 95) dB	**15.38 dB**
Bandwidth	4.15 GHz	275MHz	2.87 MHz	32 MHz	**2.344 GHz**
Power consumption	14.7mW	36mW	4mW	6.5 mW	**1.803mW**

Table .1 VGA stage-1 comparison with reference papers.

From the Table.1we can conclude that designing of Stage-1VGA in 130nm CMOS Technology is better and good in terms of -3dB frequency is 2.344GHz and power consumption is only 1.803mW. The supply voltage required is 1.8v.

B. VGA STAGE-2&3:

The stage-2 & 3 VGA has designed for the 2.4 GHz having the design specifications i.e. considering the $I_2 = 1mA$and $I_3 = 1mA$. The negative miller capacitors (C_{c2a} and C_{c2b}) are chosen to be 0.01pF in order to reduce the Miller Effect. The common mode resistors (R_{CM3} and R_{CM4}) are chosen 1MΩ each for the proper gain correction. Fig.5.2.1 shows the gain of stage-2 & 3 versus the frequency. Note that the variable gain is about (4.43 - 15.14) dB. The -3 dB bandwidth of stage-2&3 is around 2.398GHz and the power consumed in the circuit is 1.832mW. The Table.2 gives the performance comparison of present work with reference papers.

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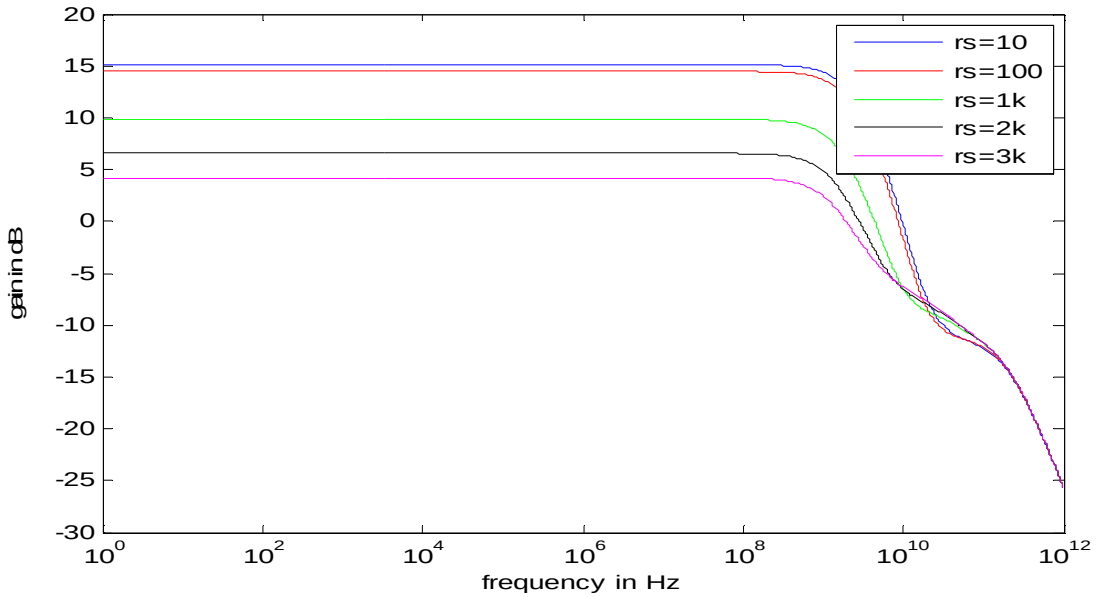

Fig.4 Gain (dB) of stage-2&3 VGA versus frequency (Hz).

Parameters	[3]	[6]	[7]	[8]	**This work**
CMOS Technology	90nm	65nm	135nm	180nm	**130nm**
Supply Voltage	1v	1.2v	1.2v	1.8v	**1.8v**
Gain(dB)	35dB	(9-43)dB	(0-60)dB	(47.5 - 95) dB	**(4.43 – 15.14)dB**
Bandwidth	4.15 GHz	275MHz	2.87 MHz	32 MHz	**2.398 GHz**
Power consumption	14.7mW	36mW	4mW	6.5 mW	**1.832mW**

Table.2VGA stage-2&3 comparison with reference papers

From the Table.2, we can prove that the gain can be variable of (4.43 – 15.14)dB this can be achieved due to the different values of R_S. The main focus of using $R_S$in thedesign is to make variable the gain. The maximum bandwidth that we achieved is 2.398 GHz and the power consumed is only 1.832mW.

V. CONCLUSION

This paper first explained the idea behind Synthetic Aperture Radar (SAR) since the VGA was to be used within such a system. Additional details about the receiver architecture for SAR were also provided. In the section-2&3, the basic requirements such as Common-Source Amplifier and Differential Amplifier were needed to design VGA. Because of using Differential Amplifier with active load the Wider Bandwidth can be achieved as for the receiver design requirements. In the section-4.1 Stage-1 VGA has designed for 2.344 GHz bandwidth, 15.38dB of gain

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and power consumption was 1.803mW all these were presented which were extracted from the system requirements for the receiver. The section-4.2 presents variable gain of (4.43 – 15.14) dB, Bandwidth was 2.398 GHz and the power dissipation was 1.832mW. All these simulations were done using 0.13um technology level-54 model files on HSPICE Simulator.

VI. ACKNOWLEDGEMENT

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BIOGRAPHY

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